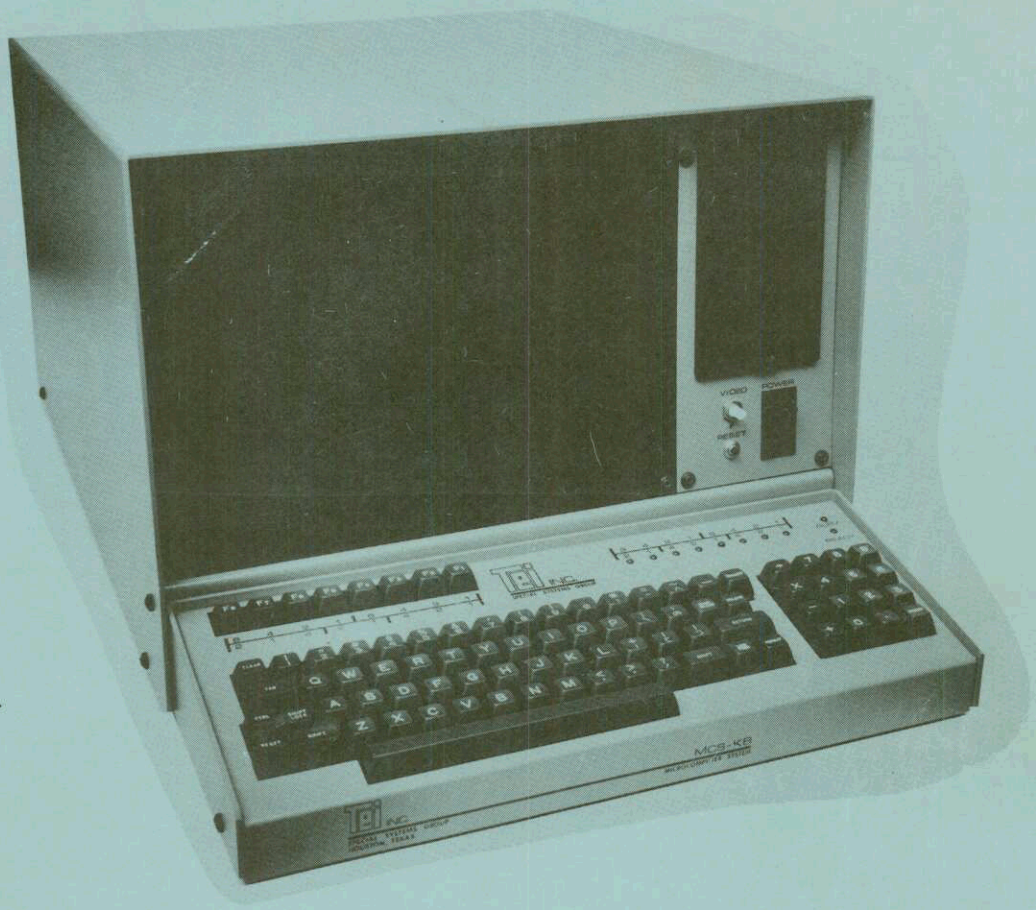
TEI INC.

SPECIAL SYSTEMS GROUP
HOUSTON, TEXAS

MCS
MICROCOMPUTER SYSTEM



TEI MCS-PT212 COMPUTER SYSTEM
USER'S MANUAL

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TEI INC.

TEXAS ELECTRONIC INSTRUMENTS, INC
5075 SOUTH LOOP EAST
HOUSTON, TEXAS 77033

WARRANTY REGISTER

Dealer/Consumer:

The information below must be filled out completely by the purchaser of this product and returned to TEI, Inc. to validate the guarantee for the specified warranty period. TEI, Inc. must have this informatiom on file before warranty repairs will be performed. Note: The "TEI, INC. SOFTWARE LICENSING AGREEMENT" must also be filled in and returned before software updates can be received.

Thank you for your business
TEI, Inc.
Special Systems Group

Purchaser Data:

Name: _____

FOLD IN

Address: _____

_____

Purchased from (Dealer) City State Zip

Product(s)	Model:	Serial No:	Date Purchased:
	_____	_____	_____
	_____	_____	_____
	_____	_____	_____
	_____	_____	_____
	_____	_____	_____
	_____	_____	_____

Software:

CPM	_____	_____
BASIC	_____	_____
FORTRAN	_____	_____
COBOL	_____	_____

TEAR OFF AT PERFORATION

FOLD IN

To help us better meet market needs please fill in following:

1. Is this your first computer? ☐ Yes ☐ No
2. For what function(s) did you purchase this system?
   ☐ Inventory ☐ Accounts receivable ☐ Word processor
   ☐ Payroll ☐ Accounts payable ☐ Other _____
3. What size memory is in your system? _____ Capacity
4. Do you wish to expand memory size in future? _____ desired? _____
5. Do you want to become a member of TEI's user group?
   ☐ Yes ☐ No ☐ What is it?
6. What specific application areas would you like to see software programs for? _____

FOLD AT MARKS, WITH ADDRESS OUT. TAPE FLAP, AND MAIL

TEI FORM NO. 189

First Class
Permit No.
12419
Houston, Texas

BUSINESS REPLY MAIL

NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

TEI INC.

TEXAS ELECTRONIC INSTRUMENTS, INC
5075 SOUTH LOOP EAST
HOUSTON, TEXAS 77033

SOFTWARE LICENSING AGREEMENT

IMPORTANT: Before opening the TEI Diskette package, please read below:

The purchaser of this TEI Software Package must read the following agreement and sign the licensing contract below. If you do not agree to the contract, you may return the Software Package to your distributor if the Diskette package is unopened.

The return of this document also registers your system, and qualifies user to receive (1) updates, (2) access to user's library, and (3) validates product warranty.

TEI, INC. SOFTWARE LICENSING AGREEMENT

The purchaser below agrees that it is receiving a copy of TEI, Inc. Software Package for use only on the computer system as designated below. The purchaser agrees that all copies will be strictly safeguarded against disclosure to, or use by persons not authorized by TEI, Inc. to use TEI, Inc. Software, and that the location of all copies will be reported to TEI, Inc. at TEI's request. The purchaser agrees that copying or unauthorized disclosure will cause great damage to TEI, Inc. and this damage is far greater than the value of the copies involved. The purchaser agrees that this agreement shall inure to the benefit of any third party holding any right, title or interest in the TEI, Inc. Software or any software from which it was derived.

FOLD

TEAR OUT AT PERFORATION

Purchaser: _____
Signature

NAME: _____ DATE: _____

FOLD

STREET: _____

CITY: _____ STATE: _____ ZIP: _____

SYSTEM MODEL: _____ SYSTEM S/N: _____

DATE PURCHASED: _____ DEALER: _____ PURPOSE: _____

SOFTWARE PACKAGE: _____

SOFTWARE S/N: _____

Fold & tape for mailing.

Make copy of agreement before mailing, if desired.

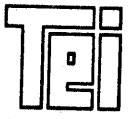
TEI Form No. 191

FOLD AT MARKS, WITH ADDRESS OUT, TAPE FLAP, AND MAIL

First Class
Permit No.
12419
Houston, Texas

BUSINESS REPLY MAIL

NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES



TEXAS ELECTRONIC INSTRUMENTS, INC
5075 SOUTH LOOP EAST
HOUSTON, TEXAS 77033

PT MANUAL CONTENTS

SECTION I:	GENERAL DATA & TEI, INC. POLICY INFORMATION
SECTION II:	MAINFRAME HARDWARE
SECTION III:	KEYBOARD
SECTION IV:	CPU PLUG-IN BOARD
SECTION V:	I/O 3P + 3S PLUG-IN BOARD
SECTION VI:	FDC PLUG-IN BOARD
SECTION VII:	RAM 16K PLUG-IN BOARD
SECTION VIII:	VCB PLUG-IN BOARD
SECTION IX:	MINI-FLOPPY DISK DRIVE (400 SERIES)
SECTION X:	FLOPPY DISK DRIVE (800 & 850 SERIES)

TEI INC.

5075 S. Loop East
Houston, Texas 77033

713-738-2300
TWX: 1-910-881-3639

SECTION I
TEI INC. PROCESSOR TERMINAL
GENERAL DATA
TEI INC. POLICY INFORMATION

SECTION I REVISED
12/20/78
P/N 13686-1

SECTION I

TEI, INC. PROCESSOR TERMINALS

TABLE OF CONTENTS

		PAGE
1.1	Introduction	1-2
1.1.2	System Contents	1-3
1.2.1	Receiving Inspection	1-4
1.2.2	Warranty Information	1-4
1.2.3	Replacement Parts & Repair Service	1-5
1.3	Precautions Before Turn-On	1-6

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SECTION 1

GENERAL DATA & TEI, INC. POLICY INFORMATION

1.1.0 INTRODUCTION

1.1.1 THE TEI, INC. PROCESSOR TERMINALS (PT112 & PT208) are complete, self-contained computer systems with CRT display, mass storage, and a full keyboard.

The CRT monitors are high resolution displays and the detached keyboard provides full upper and lower case ASCII with eight programmable special function keys. The keyboard also has status indicators to show computer BUSY or READY, and a 16-key numeric cluster pad. (Refer to "Keyboard" section of this manual for additional data.)

The Shugart SA-400 mini-floppy disk drive(s) are soft-sectored with a formated capacity of approximately 90 KB with IBM compatibility.

The printed circuit boards are all built on high grade epoxy glass to meet rigid professional standards. All boards are double-sided with plated thru holes & solder mask on both sides. Each card is equipped with card ejectors and gold plated edge connectors.

THE PC BOARDS INCLUDE:

- 8080A CPU & Z80 board special "jump to" feature.
- 16K STATIC RAM memory boards with selectable address assignment.
- INPUT/OUTPUT BOARD has three parallel ports and three serial ports with selectable baud rates of 75 to 19,200 and RS-232 and TTl outputs.
- A VIDEO CONTROLLER BOARD provides support for the 24 X 80 video display.
- THE FLOPPY DISK CONTROLLER BOARD will handle up to eight drives.
- The MAINFRAME is a heavy duty aluminum cabinet with a CVT* power supply, eight or twelve slot motherboard, and fan with washable filter.
- The same high quality which you can see in the hardware is also to be found in TEI, Inc.'s software package. The TEI, Inc. CP/M disk operator system and disk extended Basic software packages are available seperately.

*Constant Voltage Transformer - Contact TEI or your dealer for additional information on TEI'S custom CVT transformers and application notes.

1.2.1 RECEIVING INSPECTION

Immediately upon receiving your TEI product inspect all contents for damage which may have occured during shipping. If your order arrives damaged or incomplete contact your dealer so that he can take appropriate action. For further information on replacement and repair, see section 1.2.3.

1.2.2 WARRANTY INFORMATION

All components sold by TEI, Inc. are purchased through normal factory distuibution and any part which fails because of defects in workmanship or material will be replaced at no charge during the warranty period. The defedtive part must be returned post paid to TEI, Inc. within the warranty period.

GUARANTEE

TEI, INC., guarantees every computer product sold by them or their authorized representatives to be free of defects in material and workmanship, and that they will perform to rated specifications for the period indicated below from original delivery. Obligation under this guarantee is limited to the repair or replacement of the product within the warranty period, that is returned to us by the original purchaser, transportation charges prepaid, which upon our examination proves to be defective. This guarantee applies to the original purchaser, or, in the case of an original equipment manufacturer or dealer, to the end purchaser of the equipment using the product.

Field repairs may be handled by qualified, factory authorized service personnel, and the defective parts returned for replacement by the manufacturer. Details of the failure, and the part which failed, must accompany the request for repair or replacement. No warranty regarding suitability for an intended application is expressed nor implied. TEI, INC., assumes no liability for consequential damages, directly nor indirectly.

The following warranty periods apply:

Computer mainframe:	1 Year
Plug-in boards:	90 days
Video monitors:	90 days
Disk drives:	90 days
Printer:	90 days

TEI INC.

TEXAS ELECTRONIC INSTRUMENTS, INC.

1.2.3 REPLACEMENT PARTS AND REPAIR SERVICE

In order to expedite repair or replacement and return of the product contact TEI, Inc. Customer Service for a Return Authorization Number. This number should be shown on the outside of the shipping container and on the packing slip. Your product will thus be repaired and processed with the best efficiency possible and returned to you F.O.B., TEI, Inc. Houston, Texas per your shipping instructions. If method of return shipment is not specified, the product will be returned to you by the same method it was received.

At the time a return authorization is obtained from Customer Services, please provide the following information:

A. Product Model Number
B. Product S/N (if returning a module within a TEI, Inc. product indicate the product S/N).
C. Nature of Failure of Damage
D. Carrier and Waybill Number
E. Requested Return Date of Product
F. Return Carrier

Every effort was made to produce the product for high quality and reliability and was tested to specification before shipment to you. Title to the product passes to the buyer at the time of shipment and any claims for freight damage must be filed with the freight carrier promptly. TEI, Inc. makes no warranties expressed or implied against physical abuse or neglect, including freight damage. Freight damaged products may be returned to TEI, Inc. for estimates of cost to repair and replace. Such units should be returned following the procedures outlined above. A Purchase Order or letter is necessary however to cover the cost to repair or of replacement of damaged units and can form the basis of your claim for liability of the carrier. Every effort is made, utilizing professional packaging techniques, to minimize the possibility of freight damage.

1.3 PRECAUTIONS BEFORE SYSTEM TURN-ON

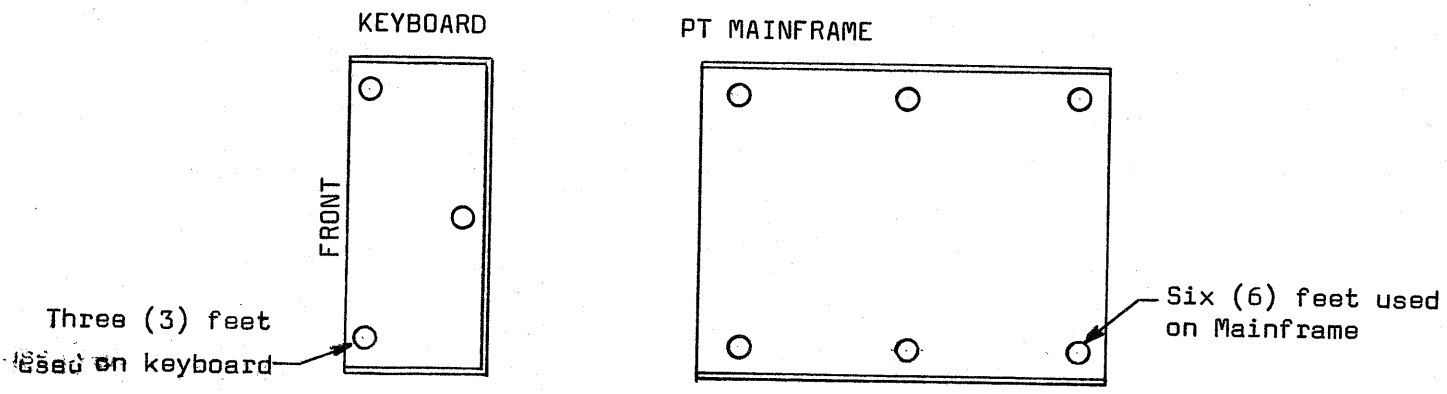
1.3.1 WARNING

BEFORE APPLYING POWER TO THIS SYSTEM, OPEN REAR PANEL AND REMOVE PLASTIC PACKING MATERIAL. ALSO CHECK THAT ALL PC BOARDS ARE PROPERLY PLUGGED IN.

NOTE: PARTIALLY PLUGGED IN BOARDS (OR BOARDS LOOSENED DURING SHIPPING) CAN CAUSE SEVERE DAMAGE TO SYSTEM COMPONENTS.

AFTER REPLACEMENT OF REAR PANEL, BE SURE KEYBOARD CABLE IS PLUGGED INTO THE CORRECT CONNECTOR.

1.3.2 Attach the self-adhesive rubber feet (supplied unmounted) to bottom surfaces of keyboard & PT mainframe in approximate position shown below



BOTTOM VIEW

TEI INC.

5075 S. Loop East
Houston, Texas 77033

713-738-2300
TWX: 1-910-881-3639

SECTION II
TEI INC. PROCESSOR TERMINAL
MAINFRAME HARDWARE

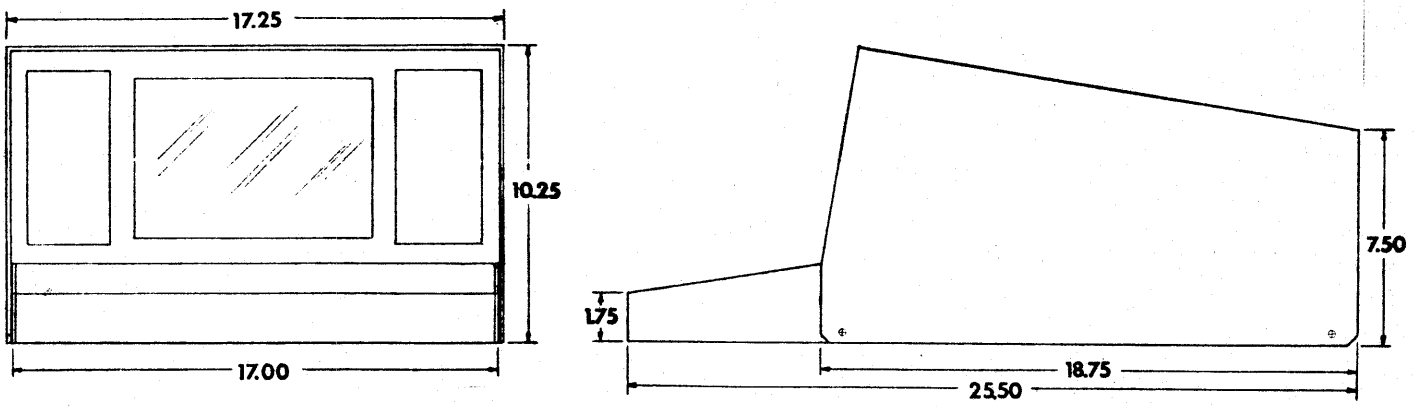
SECTION II REVISED
12/20/78
P/N 13686-2

SECTION II

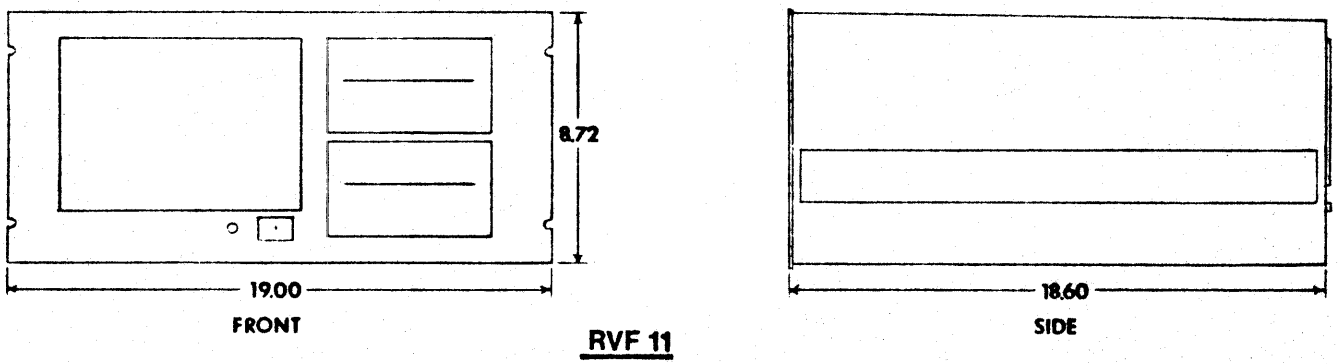
SYSTEMS MAINFRAME HARDWARE

		PAGE
2.1	PT208 (Typical for PT008, PT108, and PT408*) RVF11	2-2
2.2	PT112A (Typical for PT012A, PT212A,* PT312A,* and PT412A*)	2-5
2.3	MTS12, RTS12	2-9
2.4	MTS22, RTS22	2-11
2.5	TF12/S, RF12/S	2-14
2.6	Power Supply PC Boards	
	#13380 (PT & RVF)	2-17
	#13120 (MTS/RTS12)	
	#13130 (MTS/RTS22	2-18
	#13710 (TF/RF12)	2-19
2.7	Mother Boards - 8, 12, & 22 Slot	2-20

* Also uses a MCS-DFD (PT-412 uses two MCS-DFD units). Refer to Section X.



MCS - PT 208



RVF 11

PT208 SERIES/RVF 11
SPECIFICATIONS

NOTE: PT (Processor Terminal) is the table top version.

RVF (Rack-Video-Floppy) is the rack mount version.

SIZE: PT Units: 17.25 W X 10.25 H X 25.50 Dp. (18.75 Dp. with remote keyboard)

RVF Units: 19.00 W X 8.75 H X 19.00 Dp.

FEATURES: 9"CRT with 24 X 80 Green phosphor display

8-Slot mother board in **PT Units (Table Top** Version)

12-Slot mother board in RVF Units (Rack Mount Version)

2-SA400 Mini-Floppy Drives

PARTS LIST

REF DES	DESCRIPTION	TEI P/N
	CHASSIS MOUNTED PARTS	
BL1	FAN	2610-003
C1	Cap 45,000MF, 15VDC	1521-068
C2	Cap 26,000MF, 30VDC	1521-070
C3	Cap 10,000MF, 30VDC	1521-088
C9	Cap 3MF, 660 VAC	1543-006
CRT	Video Monitor 9"	2015-002
	Drive A,B Disk Drive	2010-001
F1	Fuse, 5A 250V 3AG	5173-022
J1	Socket Housing, 10 CRT	2122-012
J2	Socket Housing, 6 CRT	2122-010
J3	Socket Housing, 8 CRT	2122-011
J4,J5	Socket Housing, 3 CRT	2122-026
J6	Socket Housing, 2 CRT	2122-021
PCB1	* Power Supply	13380
PCB2	* Mother Board (PT UNITS)	13630
PCB2	* Mother Board (RVF UNITS)	13620
SW1	Power Switch	5113-001
T1	Transformer (60Hz)	13574
T1	Transformer (50Hz)	13605
TB1	Term. Strip, 2 POS	2171-061
	Boot, Rubber AC Cap	1592-003
	Card Guide	1750-004
	Fan Filter	13146
	Feet, Rubber (PT Only)	1419-001
	Power Cord	6080-008

REF DES	DESCRIPTION	TEI P/N
	PT 208 INTERCONNECT CABLE	
	FDC Cable (PT Units)	13614-1
	FDC Cable (RVF Units)	13614-2
	I/O Cable	13529
	KB Cable (PT Only)	13534-1
	VCB Cable	13657
	PLUG-IN PC BOARD	
	FDC Board	13340
	I/O Board	13260
	VCB Board	13390
	16K RAM Board (4200)	13420
	CPU Board	13280

* SEE pp 2-17 & 2-20 for PC Board data

REVISIONS					
ZONE	LTR	EO NO.	DESCRIPTION	DATE	APPROVED
	A	—	REDRAWN FOR CLARITY	10-5-78	

115 VAC INPUT:
CONNECTED AS SHOWN.

220 VAC INPUT:
(1) REMOVE JUMPERS TB1-1 TO 3 AND TB1-2 TO 4.
(2) JUMPER TB1-2 TO 3 AND SW1 CONN. DO NOT CHANGE.

T1 13574 (60 HZ)
13605 (50 HZ)

TB1-1 RED 1A
TB1-2 WHT 2A
TB1-3 BLK 1
TB1-4 WHT 2

SW1
F1 5A 3AG 250 V
BLK
WHT
GRN
FAN

115 VAC 50 HZ ONLY OR 60 HZ ONLY (DEPENDING ON TRANSFORMER)

C9 3MF 660VAC

PB1 P/N 13380
POWER SUPPLY PCB

J1
CR1
J2-1
45,000 MF C1
R1
J2-5

CR2
26,000 MF C2
R2
J2-2

CR3
CR4 CR5 CR6 CR7
10,000 MF C3
R3
J2-3
J2-6

U1 7812 C4
U2 7805 C5
U3 7812 C6
U4 7805 C7
U5 7812 C8

J4-
+12
+5
GND
DRIVE 1

J5-
+12
+5
GND
DRIVE 2

J6
+12
GND
9" MONITOR

J3-
F1
+8V 15A
COM
F2
+16V 2A
CHASSIS GND
F3
-16V

MOTHER BOARD P/N 13620 (FOR RVF II)
P/N 13630 (FOR PT 208)

+16V
+8V
R13 180Ω
R14 10Ω
R15 130Ω
Q2 2N3906
Q3 TIP29
R11 75Ω
R12 180Ω
C1 10MF 20V
C2 1MF
U1
C3 1MF
R10 75Ω
Q4 TIP30
Q1 2N3904
J1
CR1 IN5221
R16 130Ω
-16V

C5 C7 C9 C11 C4 C6 C8 C10 C12
C4 THRU C12 10 MFD 20 VDC

R1-1 180Ω TYP
R9-11

U1 LM301AP

CR1 R712 VARO
CR2 THRU CR7 60S4 IR
R1 THRU R3 820Ω 1/2 W
C4 THRU C8 10 MFD 20 VDC
F1 20 AMP
F2, F3 5 AMP

NOTES:

QTY	PART NUMBER	DESCRIPTION	MANUFACTURER	CODE IDENT	REF DES	ITEM

PARTS LIST

PT 208	
RVF II	
NEXT ASSY	USED ON
APPLICATION	

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.X ± .06
.XX ± .02
.XXX ± .010
ANGULAR ± .5 DEG

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

MATERIAL

CONTRACT NO.

SIGNATURES	DATE
DR Joe Beachman	10-5-78
DES	
CHK	
ENGR E. McCain	12-14-78
APP Wallace Berry	
APP	

TEXAS ELECTRONIC INSTRUMENTS, INC
HOUSTON, TEXAS

PT 208 / RVF II
SCHEMATIC

SIZE	CODE IDENT NO.	DWG NO.	REV
C	33179	13361	A
SCALE	REL EO NO.	SHEET 1 OF 1	

DWG NO. 13361 REV A

PT 112
SPECIFICATIONS

SIZE: 17.25 W X 12.75 H X 27.50 D

FEATURES: 15" CRT with 24 X 80 Green Phosphor Display

12 Slot Mother Board

1 SA400 Mini-Floppy Drive

Detachable Keyboard

PARTS LIST

MCS-PT112 A

Field Replaceable Components

REF DES		DESCRIPTION	TEI P/N
		Chassis Mounted Parts	
PB1	*	Power Supply PCB	13380-02
PB2	*	Mother Board 12 Slot	13620
T1		Transformer (60Hz)	13574
(T1)		Transformer (50Hz)	13605
C4		Cap, 3MF @660 VAC	1543-006
PCB3-J2			
Drive 1-J2			
		Socket Housing, 4 CKT	2122-009
PCB3-J1		Socket Housing, 6 CKT	2122-010
PCB1-J1		Socket Housing, 8 CKT	2122-011
PCB2-J1		Socket Housing, 2 CKT	2122-021
CRT.			
Conn.		Connector, 4 Pin	2125-017
TB1		Terminal Strip, 2 Pos	2171-061
Fan		Fan	2610-003
-		Filter, Fan	13146
SW1		Power Switch	5113-001
SW2		Reset Switch	5110-005
F1		Fuse 5A 250V, 3AG	5173-062
CRT		Video Monitor, 15"	2015-001
Drive 1		Minifloppy Disk Drive	2010-001
-		Power Cord	6080-008
-		Rubber Feet	1419-001
XF1		Fuse Holder	5161-002
-		Boot, Rubber Cap	1592-003
-		Card Guide	1750-004
-			
-		Screw 6-32 X 3/8 BLK	2800-025

REF DES	DESCRIPTION	TEI P/N
	INTERCONNECT CABLES	
-	FDC Cable (PT112,PT312)	13566
-	I/O Cable KB	13529
-	KB Cable	13534
-	CRT Cable	13567
-	FDC Cable (PT212,PT312)	13425
-	FDC Cable (PT412)	13837
	PLUG-IN PC BOARDS	
-	CRT Controller	13390
-	FDC Board	13340
-	I/O Board	13260
-	16K RAM 4200	13420
-	CPU Board	13281

* See pp 2-17 & 2-20 for PC Board

PT-012A Stripped-down version of PT-112A with only power supply, mother board, CRT monitor and cover over space normally occupied by the SA-400 drive.

PT-112A As described on preceding page.

PT-212A A TEI MCS-DFD* unit is used for the mass storage. Mini-Drive is not used.

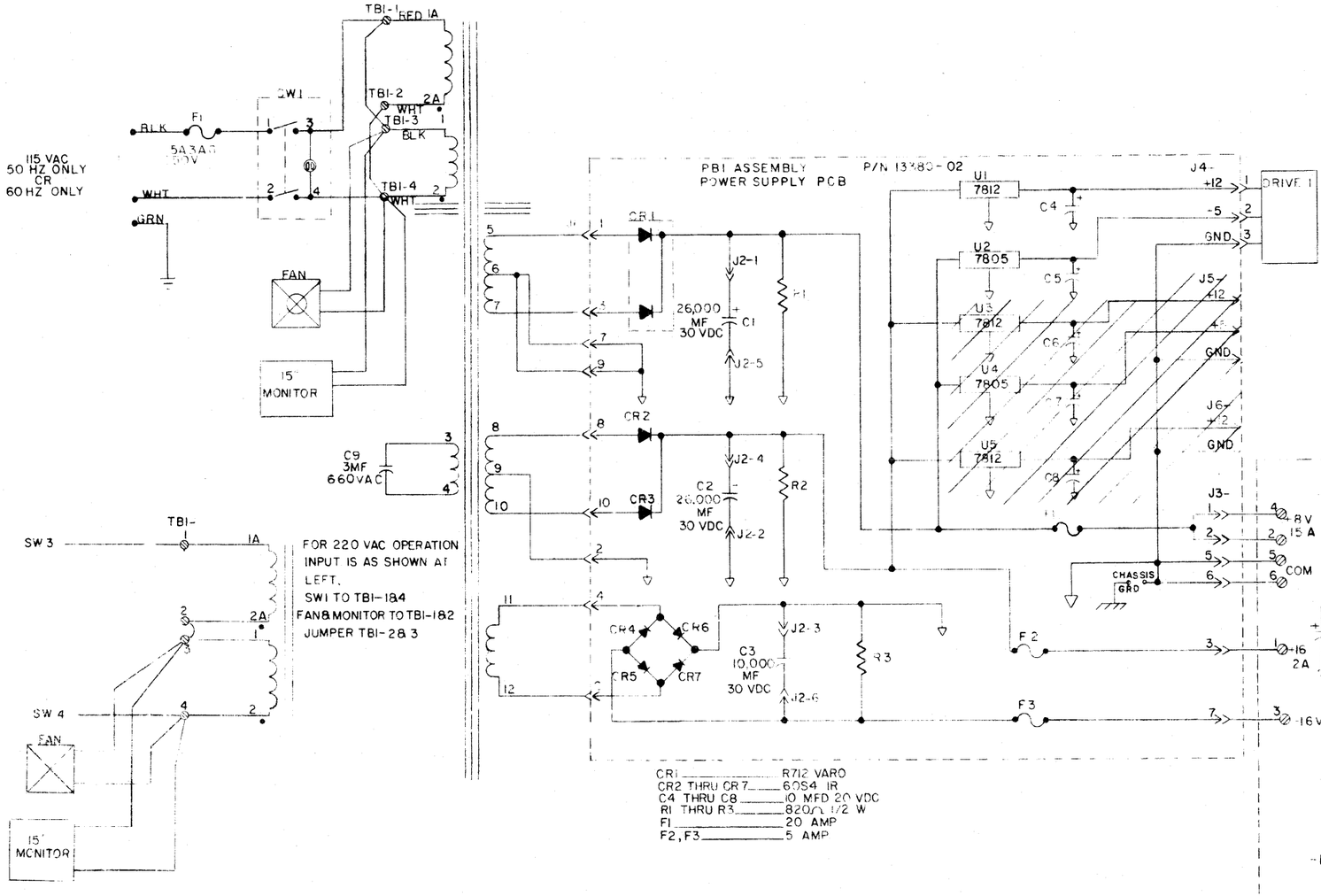
PT-312A Same as PT-212A above except that Mini-Drive is installed for a mixed drive system.

PT-412A The PT-112A unit (less the Mini-Drive) has two MCS-DFD* units for mass storage (four SA-800 or SA-850 drives).

*Refer to section X for data on MCS-DFD.

REVISIONS					
ZONE	LTR	EO NO.	DESCRIPTION	DATE	APPROVED

*T1 (60 HZ 13574)
(50 HZ 13605)



CR1	R712 VARO
CR2 THRU CR7	60S4 IR
C4 THRU C8	10 MFD 20 VDC
R1 THRU R3	820Ω 1/2 W
F1	20 AMP
F2, F3	5 AMP

1. CROSSED OUT COMPONENTS(ON PCB CIRCUITRY) ARE NOT USED FOR THIS APPLICATION.
2. CVT (TRANSFORMER) DESIGN IS FREQUENCY DEPENDENT.

NOTES:

(ALL PT012, PT112, PT212, PT312 UNITS MANUFACTURED AFTER 5/1/78)

QTY	PART NUMBER	DESCRIPTION	MANUFACTURER	CODE IDENT	REF DES	ITEM

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.X ± .06
.XX ± .02
.XXX ± .010
ANGULAR ± .5 DEG

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

MATERIAL

CONTRACT NO.

SIGNATURES	DATE
DR	8-28-78
DES	
CHK	
ENGR E. McClain	12-13-78
APP Wallace Berry	
APP	

TEXAS ELECTRONIC INSTRUMENTS, INC
HOUSTON TEXAS

MCS-PT112A SCHEMATIC

SIZE	CODE IDENT NO.	DWG NO.	REV
D	33179	13798	A
SCALE	REL EO NO.	SHEET 1 OF 1	

ADV A 13798 ON DWG NO

MTS 12/RTS 12
SPECIFICATIONS

NOTE: MTS (Mainframe Terminal System) is the table top version

RTS (Rackmount Terminal System) is the Rack Mount version

SIZE: (Combines the MCS 112 Mainframe with the DFD 80 & RM12 With RFD 80)

MCS 112: 17.25 W X 12.00 D X 7.25 H

DFD 80: 17.25 W X 20.00 D X 5.50 H

RM12: 19" Wide Rack Mounting X 7" High X 12.0" Deep

RFD 80: 19" Wide Rack Mounting X 7" High X 19.5" Deep

FEATURES: FDC Board to control DFD 80

2 SA800 Drives

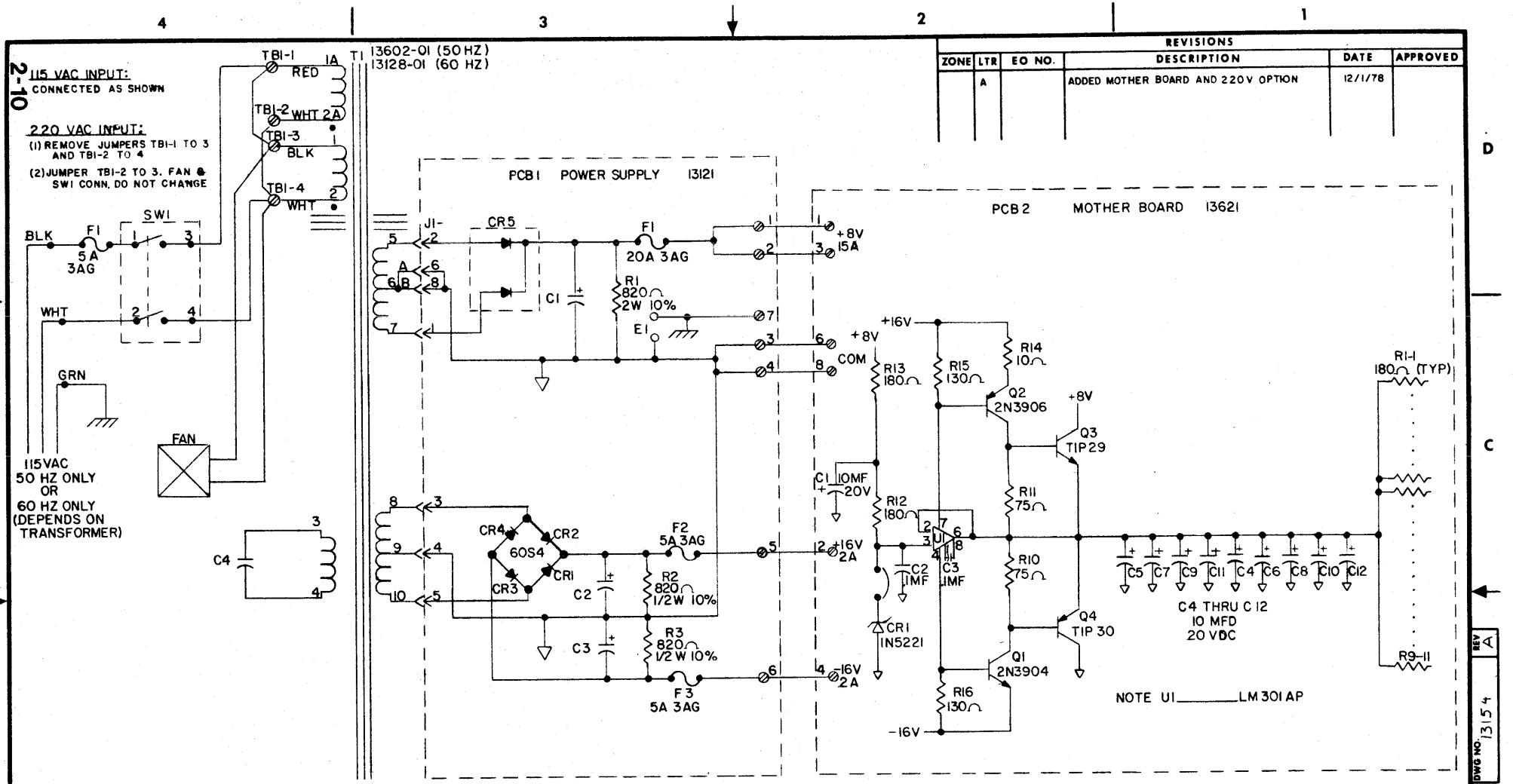
PARTS LIST

REF DES	DESCRIPTION	TEI P/N
	CHASSIS MOUNTED PARTS	
PCB2	Mother Board 12 Slot	13620
PCB1	Power Supply	13121
T1	Transformer (112-60Hz)	13128-01
T1	Transformer (RM12-60Hz)	13128-02
T1	Transformer (112-50Hz)	13602-01
T1	Transformer (RM12-50Hz)	13602-02
C4	Cap, 3MF @660 VAC	1543-006
PCB1-J1	Socket Housing, 8 CKT	2122-011
PCB2-J1	Socket Housing, 2 CKT	2122-021
Fan	Fan	2610-003
-	Filter, Fan	13146
SW1	Power Switch	5113-001
SW2	Reset Switch	5110-005
F1	Fuse 5A 250V, 3 AG	5173-062
-	Power Cord	6080-003
-	Rubber Feet	1419-001
-	Boot, Rubber Cap	1592-003
-	Card Guide	1750-004

NOTE: Refer to Section X of Manual For DFD 80 Parts List & Schematic

* Refer to pp 2-18 & 2-20 for PC Board data

REF DES	DESCRIPTION	TEI P/N
	INTERCONNECT CABLES	
-	FDC Cable	13425
-	I/O Cable	13658
	PLUG IN PC BOARDS	
-	FDC Board	13340
-	I/O Board	13260
-	16K RAM (4200)	13420
-	CPU Board	13281



REVISIONS					
ZONE	LTR	EO NO.	DESCRIPTION	DATE	APPROVED
	A		ADDED MOTHER BOARD AND 220V OPTION	12/1/78	

NOTES			
C1	45,000	15V	TEI P/N 1521-068
C2,C3	10,000	30V	TEI P/N 1521-088
C4	3 MF	600 VAC	TEI P/N 1543-006
CR1 THRU CR4		60S4	TEI P/N 4825-043
CR5 R712 VARO			TEI P/N 4815-017

NOTES:

QTY	PART NUMBER	DESCRIPTION	MANUFACTURER	CODE IDENT	REF DES	ITEM

PARTS LIST

	MCS-112
NEXT ASSY	USED ON
APPLICATION	

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.X ± .06
.XX ± .02
.XXX ± .010
ANGULAR ± .5 DEG

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

MATERIAL

CONTRACT NO.

SIGNATURES	DATE
DR Joseph B Wachtrup	11-30-78
DES	
CHK	
ENGR E. McCain	12-13-78
APP Wallace Barry	
APP	

TEXAS ELECTRONIC INSTRUMENTS, INC
HOUSTON, TEXAS

MCS-112 SCHEMATIC

SIZE	CODE IDENT NO.	DWG NO.	REV
C	33179	13154	A
SCALE	REL EO NO.	SHEET	OF

REV A
DWG NO. 13154

MTS 22/RTS 22
SPECIFICATIONS

NOTE: MTS (Mainframe Terminal System) is the table top version

RTS (Rackmount Terminal System) is the Rack Mount version

SIZE: (Combines the MCS 122 Mainframe with the DFD 80 & RM22 with RFD 80)

MCS 122: 17.25 W X 19.50 D X 5.50 H

DFD 80: 17.25 W X 20.00 D X 5.50 H

RM22: 19" Wide Rack X 7" High X 19.5 Deep°

RFD 80: 19" Wide Rack X 7" High X 19.50 Deep

FEATURES: FDC Board to control DFD 80

2 SA800 Drives

PARTS LIST

REF DES	DESCRIPTION	TEI P/N
	Chassis Mounted Parts	
PCB2	* Mother Board 22 Slot	13610
PCB1	* Power Supply	13131
T1	Transformer (122-60Hz)	13214-01
T1	Transformer (RM22-60Hz)	13214-02
T1	Transformer (122-50Hz)	13575-01
T1	Transformer (RM22-50Hz)	13575-02
C4	Cap, 5MF @660 VAC	1543-001
PCB1-J1	Socket Housing, 12 CKT	2122-013
PCB2-J1	Socket Housing, 2 CKT	2122-021
FAN	FAN	2610-003
-	Filter,Fan	13146
SW1	Power Switch	5110-001
SW2	Reset Switch	5110-005
F1	Fuse 10A 250V, 3 AG	5173-079
-	Power Cord	6080-003
-	Rubber Feet	1419-001
-	Boot, Rubber Cap	1592-003
-	Card Guide	1750-004

NOTE: Refer to Section X of Manual For DFD 80 Parts List & Schematic.

* Refer to pp 2-18 & 2-20 for PC Board data

REF DES	DESCRIPTION	TEI P/N
	INTERCONNECT CABLES	
-	FDC Cable	13425
-	I/O Cable	13658
	PLUG-IN PC BOARDS	
-	FDC Board	13340
-	I/O Board	13260
-	16K RAM (4200)	13420
-	CPU Board	13281

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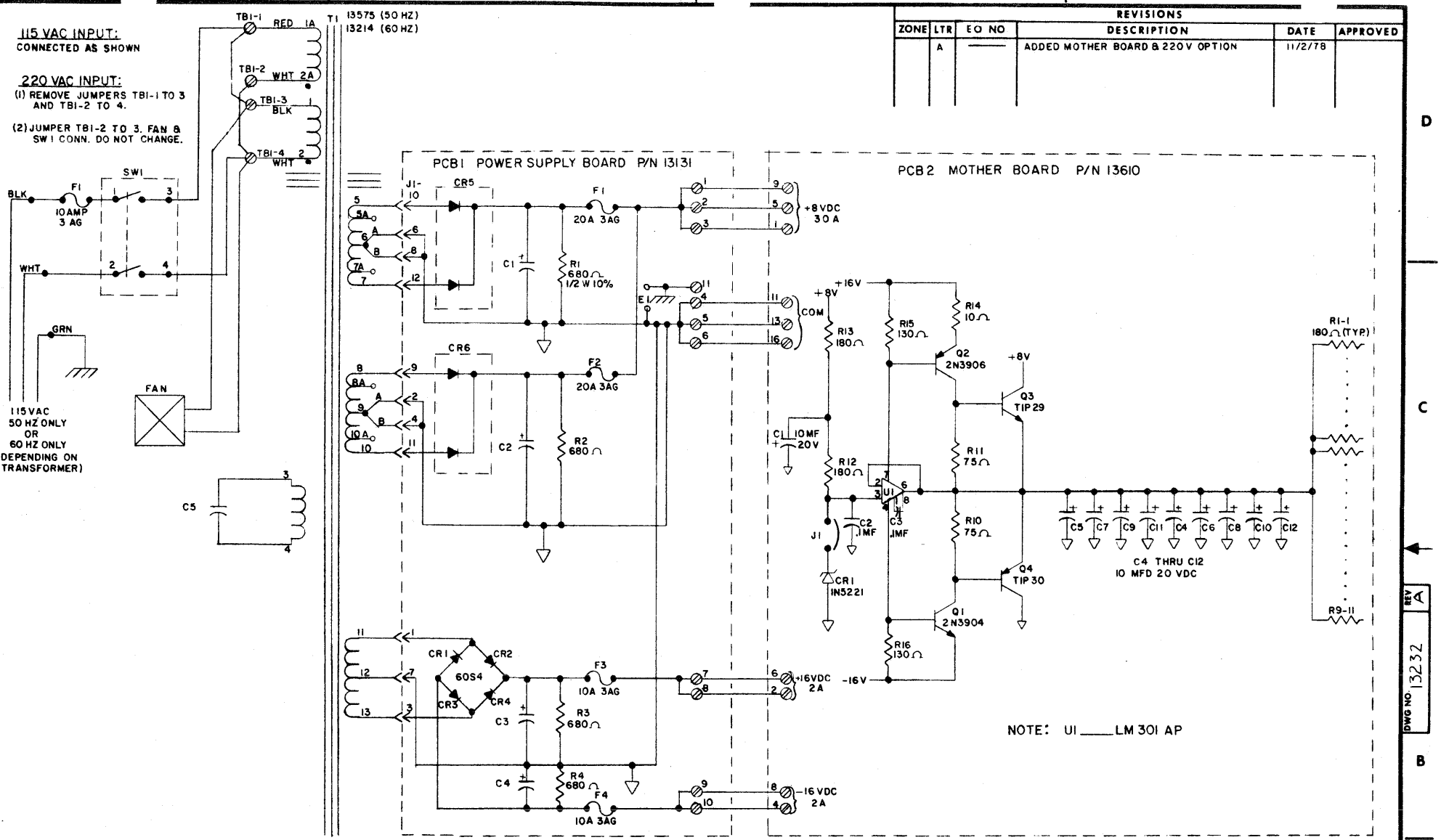


REVISIONS					
ZONE	LTR	EO NO	DESCRIPTION	DATE	APPROVED
	A	———	ADDED MOTHER BOARD & 220 V OPTION	11/2/78	

NOTES:	
C1,C2	45,000 MF, 15V TEI P/N 1521-068
C3,C4	10,000 MF, 30 V TEI P/N 1521-088
C5	5 MF, 660 VAC TEI P/N 1543-001
CR1 THRU CR4	60S4 TEI P/N 4825-043
CR5, CR6	TEI P/N 4815-017

NOTES:

QTY	PART NUMBER	DESCRIPTION	MANUFACTURER	CODE IDENT	REF DES	ITEM

PARTS LIST

	MCS-122
NEXT ASSY	USED ON
APPLICATION	

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.X ± .06
.XX ± .02
.XXX ± .010
ANGULAR ± .5 DEG

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

MATERIAL

CONTRACT NO.

SIGNATURES	DATE
DR J. BROCHTRUP	11-2-78
DES	
CHK	11-8-78
ENGR	11-8-78
APP Wallace Berry	
APP	

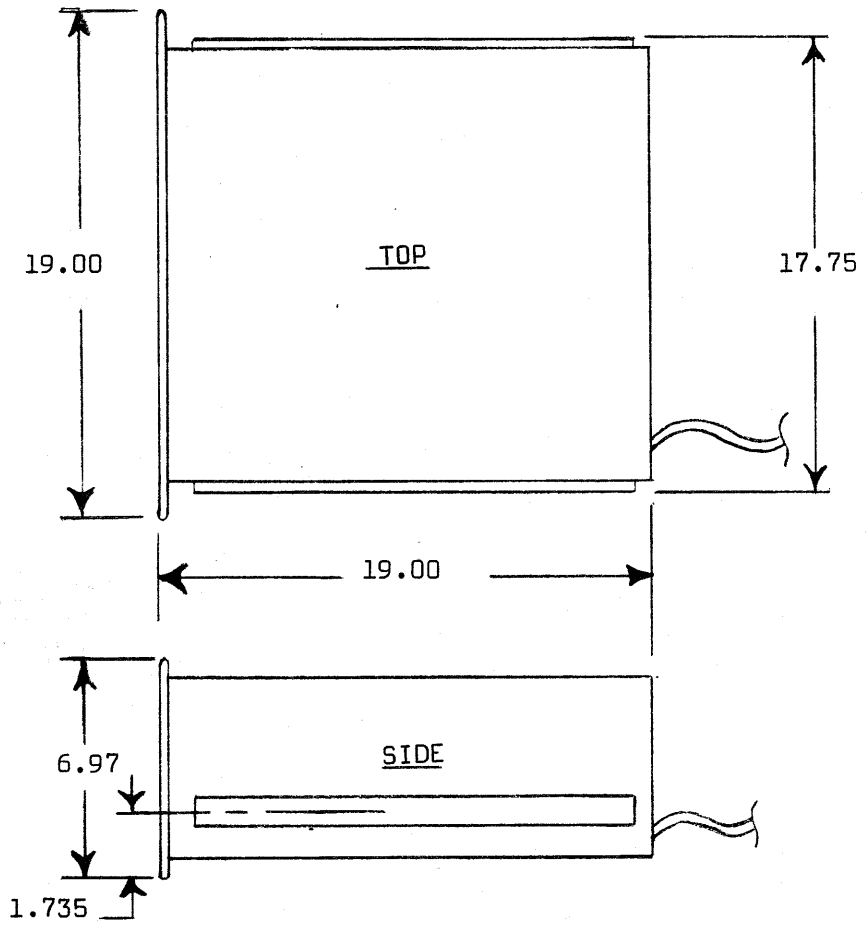
TEXAS ELECTRONIC INSTRUMENTS, INC
HOUSTON, TEXAS

MCS-122
SCHEMATIC

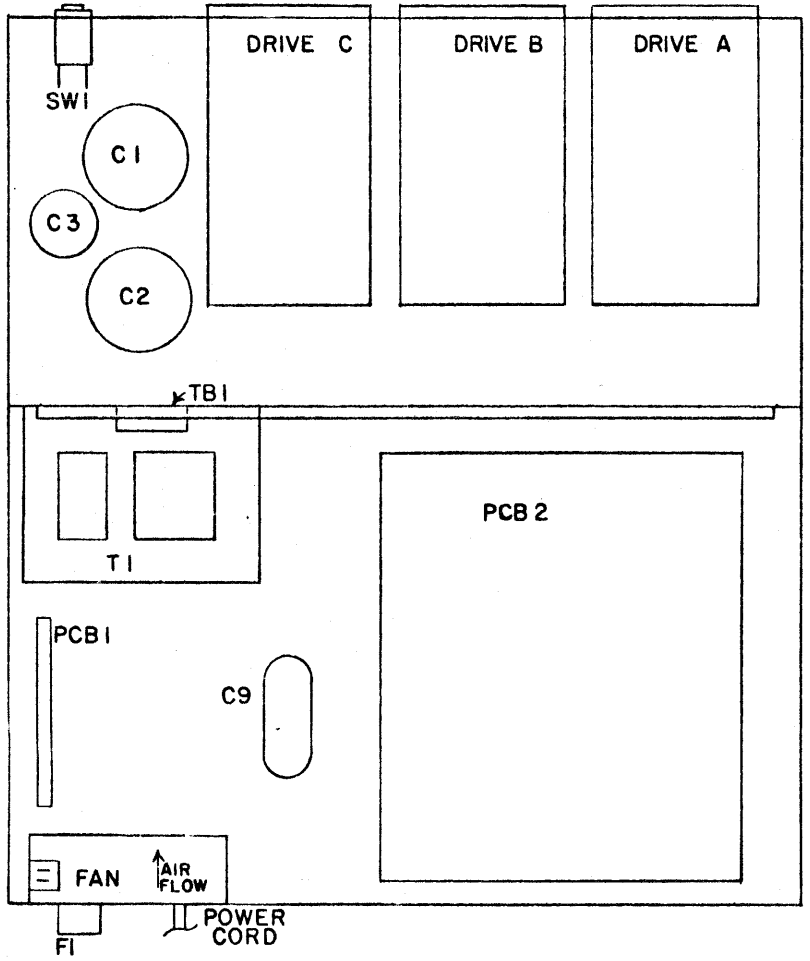
SIZE	CODE IDENT NO.	DWG NO.	REV
C	33179	13232	A
SCALE	REL EO NO.	SHEET 1 OF 1	

REV A
DWG NO. 13232

2-13



RF 12 OUTLINE DRAWING



TF-12/RF-12 Component Layout

TF 12/RF 12
SPECIFICATIONS

NOTE: TF (Triple Floppy) is the table top version

RF (Rackmount Floppy) is the rack mount version

SIZE: TF Units: 17.25 W X 7.25 H X 19.50 D

RF Units: 19.00 W X 7.00 H X 18.50 D

FEATURES: 12 Slot Mother Board

CPM, Two 16K Ram, FDC, and 3P + 3S I/O Cards

2 SA400 Drives with provisions for a 3rd Mini or a Cable connected

DFD-80 or DFD-85

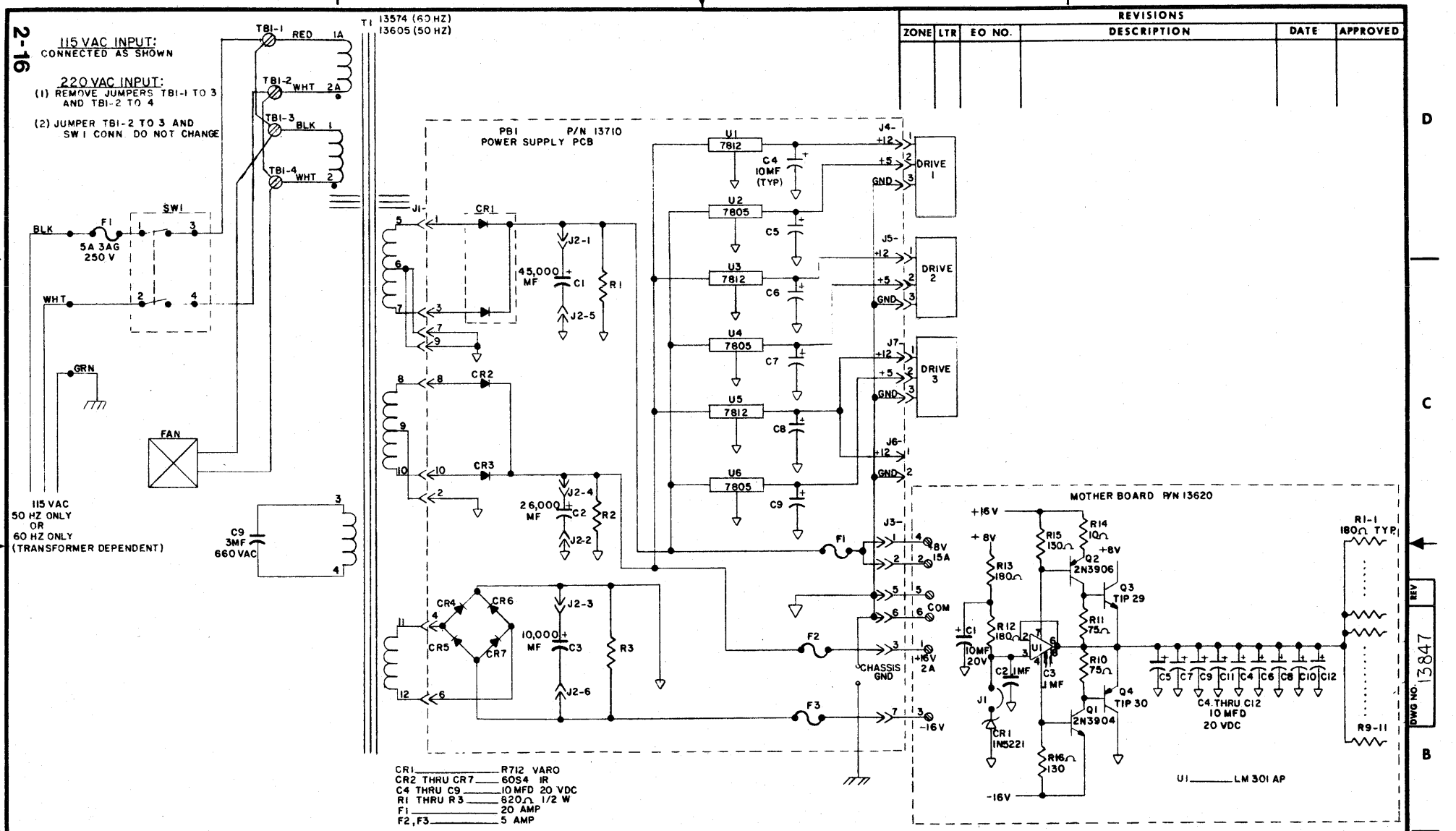
PARTS LIST

MCS-TF12/RF12

REF DES	DESCRIPTION	TEI P/N
	CHASSIS MOUNTED PARTS	
BL1	FAN	2610-003
C1	Cap 45,000MF, 15VDC	1521-068
C2	Cap 26,000MF, 30VDC	1521-070
C3	Cap 10,000MF, 30VDC	1521-088
C9	Cap 3MF, 660 VAC	1543-006
	Drive A,B,C, Disk Drive	2010-001
F1	Fuse, 5A 250V 3AG	5173-022
J1	Socket Housing, 10 CRT	2122-012
J2	Socket Housing, 6 CRT	2122-010
J3	Socket Housing, 8 CRT	2122-011
J4,J5, J7	Socket Housing 3 CRT	2122-026
J6	Socket Housing 2 CRT	2122-021
PCB1	Power Supply	13710
PCB2	Mother Board	13621
SW1	Power Switch	5113-001
T1	Transformer 60Hz Only	13574
	50Hz Only	13605
TB1	Term.Strip, 2 POS	2171-061
	Boot, Rubber AC Cap	1592-003
	Card Guide	1750-004
	Fan Filter	13146
	Feet, Rubber	1419-001
	Power Cord	6080-008

REF DES	DESCRIPTION	TEI P/N
	TF12/RF12 INTERCONNECT CABLE	
FDC Cable		13799
I/O Cable		13529
	PLUG - IN PC BOARD	
	FDC Board	13340
	I/O Board	13260
	VCB Board	13390
	16 K RAM Board (4200)	13420

NOTE: Refer to pp 2-19 & 2-20 for PC Board data, or specific section of manual for plug-in Board data



REVISIONS					
ZONE	LTR	EO NO.	DESCRIPTION	DATE	APPROVED

NOTES:

QTY	PART NUMBER	DESCRIPTION	MANUFACTURER	CODE IDENT	REF DES	ITEM

PARTS LIST

NEXT ASSY	USED ON
	MCS-TF12
APPLICATION	

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.X ± .06
.XX ± .02
.XXX ± .010
ANGULAR ± .5 DEG

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

MATERIAL

CONTRACT NO.

SIGNATURES	DATE
DR J. Brockway	9-29-78
DES	
CHK E. McCain	10-2-78
ENGR E. McCain	10-2-78
APP Wallace Berry	
APP	

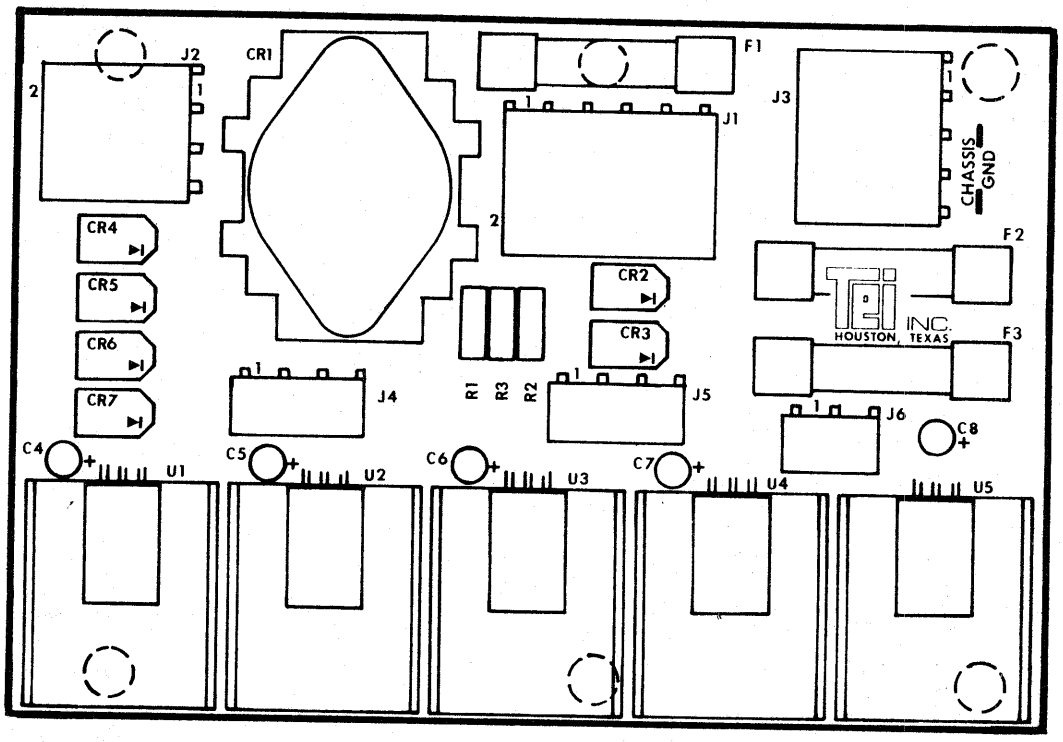
TEXAS ELECTRONIC INSTRUMENTS, INC
HOUSTON, TEXAS

MCS-TF12/RF12 SCHEMATIC

SIZE	CODE IDENT NO.	DWG NO.	REV
C	33179	13847	
SCALE	REL EO NO.	SHEET 1	OF 1

REV 13847 DWG NO

POWER SUPPLY PC BOARD #13380
(Typ. for PT-208 and PT-112 Series)



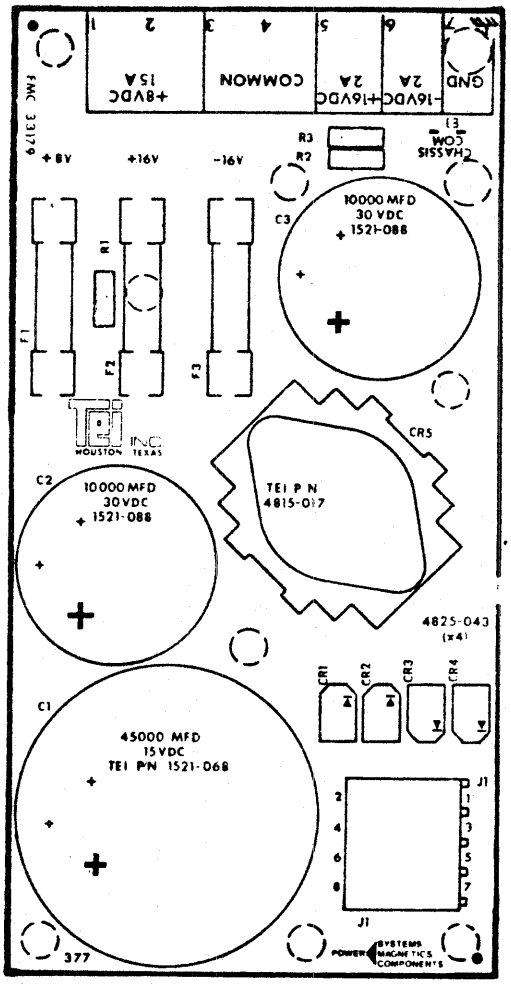
PARTS LIST

REF DES	DESCRIPTION	TEI P/N
	PCB FAB	13381
C4 THRU C8	Cap, 10MF, 20VDC	1580-001
CR1	Rectifier, Half Bridge	4815-017
CR2 Thru CR7	Diode, 3AMP	4825-043
F1	Fuse 20A, 32V, 3AG	5173-029
F2,F3	Fuse 5A,250V, 3AG	5173-022
J1	Pin Header, 10 CKT	2122-006
J2	Pin Header, 6 CKT	2122-004
J3	Pin Header, 8 CKT	2122-005
J4,J5	Pin Header, 3 CKT	2122-025
J6	Pin Header, 2 CKT	2122-020
R1,R2,R3	Resistor 850Ω 1/2W 10%	4725-329
U1,U3,U5	Regulator 7812	3120-007
U2,U4	Regulator 7805	3120-003
	Heat Sink, Regulator	4890-003
	Heat Sink, Bridge	4894-002

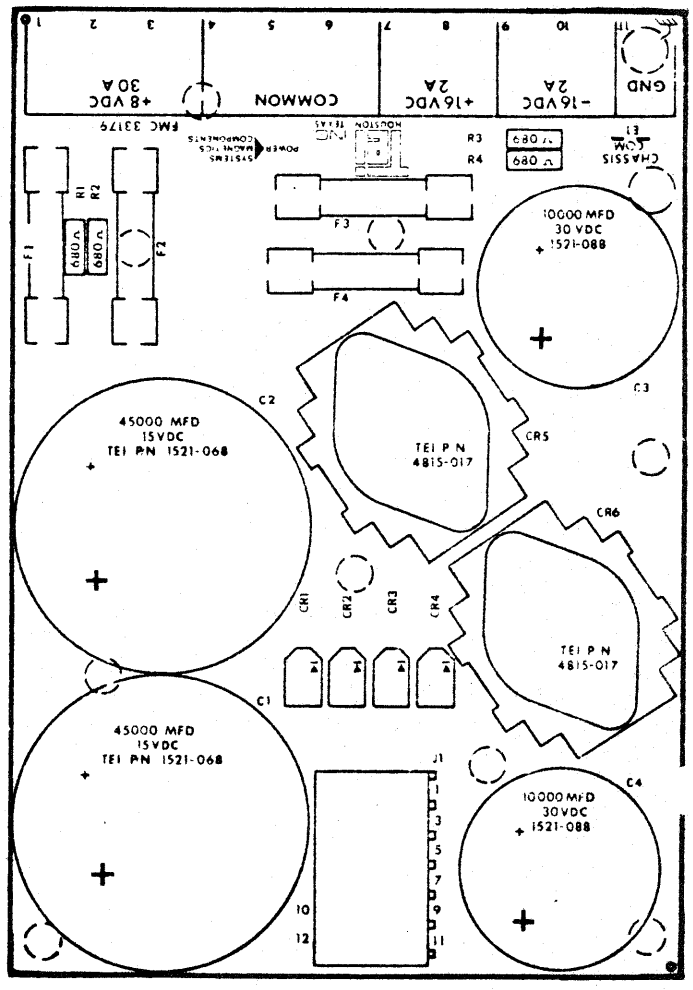
NOTE; C6,C7,C8,J5,U3,U4,U5
NOT USED ON 13381-01 (PT-112 SERIES)

POWER SUPPLY PC BOARDS
(Typ. for MTS-12 and MTS-22)

PC BOARD #13120
(MTS-12)



PC BOARD #13130
(MTS-22)



PARTS LIST

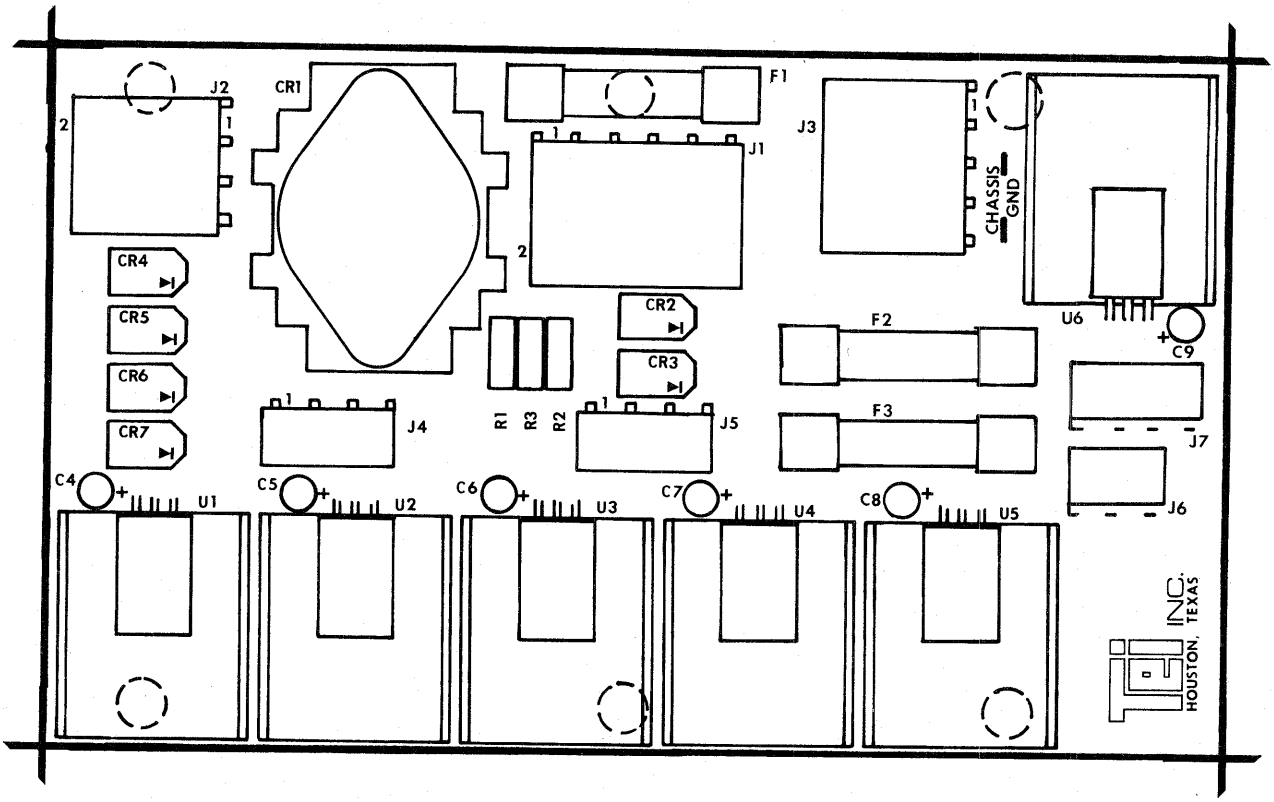
REF DES	DESCRIPTION	TEI P/N
PCB	FAB Power Supply	13121
C1	Cap, 45,000 MFD, 15 VDC	1521-068
C2, C3	Cap, 10,000 MFD, 30 VDC	1521-088
CR1 thru CR4	Diode 60S4	4825-043
CR5	Rectifier, R702	4815-017
E1	#20 Ga Jumper	6009-003
F1	Fuse, 20A, 32V, 3AG	5173-029
F2, F3	Fuse, 5A, 250V, 3AG	5173-022
J1	Pin Header, 8 CKT	2122-005
R1, R2, R3	RES 820 Ω 1/2 W 10%	4725-329

PARTS LIST

REF DES	DESCRIPTION	TEI P/N
PCB	FAB Power Supply	13131
C1,C2	Cap, 45,000 MFD, 15VDC	1521-068
C3,C4	Cap, 10,000 MFD, 30VDC	1521-088
CR1 thru CR4	Diode 60S4	4825-043
CR5,CR6	Rectifier, R702	4815-017
E1	#20 GA Jumper	6009-003
F1,F2	Fuse, 20A, 32V, 3AG	5173-029
F3,F4	Fuse, 10A, 32V, 3AG	5173-022
J1	Pin Header, 12 CKT	2122-007
R1, R2, R3,R4,	Res 680 Ω 1/2W 10%	4725-329

POWER SUPPLY PC BOARD #13710

(Typ. for TF-12 and RF-12)



POWER SUPPLY PCB		
REF DES	DESCRIPTION	TEI P/N
	PCB FAB	13711
C4 THRU C9	Cap, 10MF, 20VDC	1580-001
CR1	Rectifier, Half Bridge	4815-017
CR2 THRU CR7	Diode, 3AMP	4825-043
F1	Fuse 20A, 32V, 3AG	5173-029
F2,F3	Fuse 5A,250V,3AG	5173-022
J1	Pin Header, 10 CKT	2122-006
J2	Pin Header, 6 CKT	2122-004
J3	Pin Header, 8 CKT	2122-005
J4,J5,J7	Pin Header, 3 CKT	2122-025
J6	Pin Header, 2 CKT	2122-020
R1,R2,R3	Resistor 820Ω 1/2W 10%	4725-329
U1,U3,U5	Regulator 7812	3120-007
U2,U4,U6	Regulator 7805	3120-003
	Heat Sink Regulator	4890-003
	Heat Sink Bridge	4894-002

TEI INC.

5075 S. Loop East
Houston, Texas 77033

713-738-2300
TWX: 1-910-881-3639

SECTION III
TEI INC. PROCESSOR TERMINAL
KEYBOARD

P/N 13686-3

SECTION III

TEI, INC. MCS-KB

TABLE OF CONTENTS

		PAGE
3.1	Theory of Operation	3-2
3.2	Signal & Power Pin-Out	3-3
3.3	Parts List	3-4
3.4.1	PCB Component Layout	3-5
3.4.2	Key Pad Layout	3-7
3.5	I.C. List & Function	3-8
3.6	Schematic Diagram	3-9

MCS-KB THEORY OF OPERATION

THE MCS-KB is the KEYBOARD for the TEI MICROCOMPUTER SYSTEMS.
The keyboard requires two SERIAL PORTS and +8 & -16 volts. Functionally it has 64 keys in the standard typewriter format, a 16 key numeric cluster, eight special function keys, and eight LED'S for a special function programable display, and BUSY/READY lights for operator convenience. The 64 key pad and the 16 key cluster are on SERIAL PORT 1. This port also controls the BUSY/READY lights. SERIAL PORT 2 is used to INPUT data from the eight special function keys and to OUTPUT data to the eight special function lights.

BOTH SERIAL PORTS on the keyboard are RS-232 compatible and both are controlled by AY-5-1013 UARTS. The baud rate is user dependent in that a 16X clock must be provided by the user. When the keyboard is used with a TEI SYSTEM or in conjunction with the MCS-3P+3S I/O BOARD all proper signals are provided.

THE EIGHT SPECIAL FUNCTION KEYS may be considered as the EIGHT BITS for SERIAL PORT 2, F1 being the least significant BIT. For example, if F8 were depressed and data INPUT from PORT 2, the data would be 80H. THE EIGHT SPECIAL FUNCTION LIGHTS may be considered in the same way, only the lights indicate the BIT pattern for data OUTPUT to PORT 2.

THE BUSY/READY LIGHTS are controlled by outputting data to SERIAL PORT 1. The READY LIGHT is turned ON by outputting a "1" to Port 1, and the BUSY LIGHT is turned ON with a "2" to PORT 1.

THE 64 KEY PAD AND THE 16 KEY PAD are scanned and decoded by a AY-5-2376 KEYBOARD ENCODER. The main features of this chip are TWO KEY ROLLOVER, N-KEY LOCKOUT, and KEY DE-BOUNCE. When any key in the KEY MATRIX is closed the KEY POSITION is DECODED and the ASCII representation for that key is OUTPUT to the UART for SERIAL PORT 1. The data is then converted into a serial data word and transmitted to the I/O BOARD.

In addition to the standard keys normally found on a typewriter keyboard there are two designed to compliment the TEI SYSTEM. These are the RESET and the CLEAR. These are not scanned by the keyboard encoder and have one side connected to ground and the other to the output connector. In the TEI SYSTEM the RESET is connected to BUSS LINE 75 which will cause a HARDWARE RESET when taken LOW. The CLEAR is connected to BUSS LINE 54 which will CLEAR ALL I/O PORTS TO 0 when it is taken LOW (this also occurs when a RESET is generated).

The keyboard interfaces to the I/O BOARD through a DB-25 CONNECTOR.

3.2 THE SIGNAL AND POWER PIN-OUT IS AS FOLLOWS:

12 PIN MATE-N-LOK (PC BOARD CONNECTOR:)	25 DB CONNECTOR:	SIGNAL/POWER
PIN 1	PIN 10	-16v
PIN 2	PIN 5	RESET
PIN 3	PIN 11	POWER COMMON
PIN 4	PIN 6	CLEAR
PIN 5	PIN 8	+8v
PIN 6	PIN 7	16 X CLOCK
PIN 7	PIN 15	XMIT ASCII DATA
PIN 8	PIN 3	RCV TO SPECIAL FUNCTION LED'
PIN 9	PIN 14	RCV TO BUSY-READY LED'S
PIN 10	PIN 4	XMIT TO FUNCTION KEYS.
PIN 11	NO CONN.	CHASSIS GROUND
PIN 12	PIN 9	+16v

NOTE: ON TEI SYSTEMS THE SPECIAL FUNCTION KEYS AND LED'S ARE ON PORT FF FOR DATA AND FE FOR STATUS. THE ASCII DATA AND BUSY-READY LIGHTS ARE ON PORTS 00 FOR STATUS AND 01 FOR DATA.

TEI INC.

PARTS LIST

MCS-KB PC BOARD

REF DES	DESCRIPTION	TEI P/N
-	FAB	13251
C1, C2, C3	Cap .1MF	1562-002
C4, C5	Cap 1.0MF	1581-008
C6 Thru C10		
C12, C13	Cap .1MF	1562-002
C11	Cap 39 PF	1551-023
C14	Cap .01MF	1551-001
C16 Thru C19	Cap 10MF, 20VDC	1580-001
C20, C21	CAP .01MF, 150VDC	1551-001
C22	Cap .003MF, 1KV	1551-007
C23, C24	Cap, .1MF	1562-002
C25 Thru C27	Cap .1MF	1562-002
CR11 Thru		
CR14	Diode 1N916	4825-009
CR15, CR16	Diode 1N759	4840-011
Q1, Q3,	Transistor 2N3906	4864-007
R1 Thru R10	RES 150 Ω 1/4W 2%	4741-258
R11 Thru R18	1K 1/4W 2%	4741-337
R19	RES 10K 1/4W 2%	4725-433
R20, 21, 23	100K 1/4W 2%	4741-529
R22	RES 68K 1/4W 2%	4741-609
R24, R25	470K 1/4W 2%	4741-594
R26	470 Ω 1/4W 2%	4741-306
R27	220 Ω 1/4W 2%	4741-274
R28, R29	1K 1/4W 2%	4741-337
R30, R32	39K 1/4W 2%	4741-490
R31	47K 1/4W 2%	4741-40Z
R33, R34	1K 1/4W 2%	4741-337
R35, R36	RES 270 Ω 1/2W 10%	4725-283
R37 Thru		
R40	1K 1/4W 2%	4741-337
U1, U2	IC Chip 8212	3162-001
U3	7400	3161-018
U4, U5	7404	3161-016
U6, U7	IC Chip AY-51013	3100-013
U8	IC Chip AY5-2376	3100-014
U9	IC Chip 555	3100-001
U10	Regulator 7805	3120-003
U11	Regulator 79M12	3120-005
U12	7401	3161-0Z1
U13	IC Chip 74LS132	3164-019
U14	9617	3160-010
U15	IC Chip 9616	3160-009
R41	RES 22K Ω 1/4W 2%	4725-466

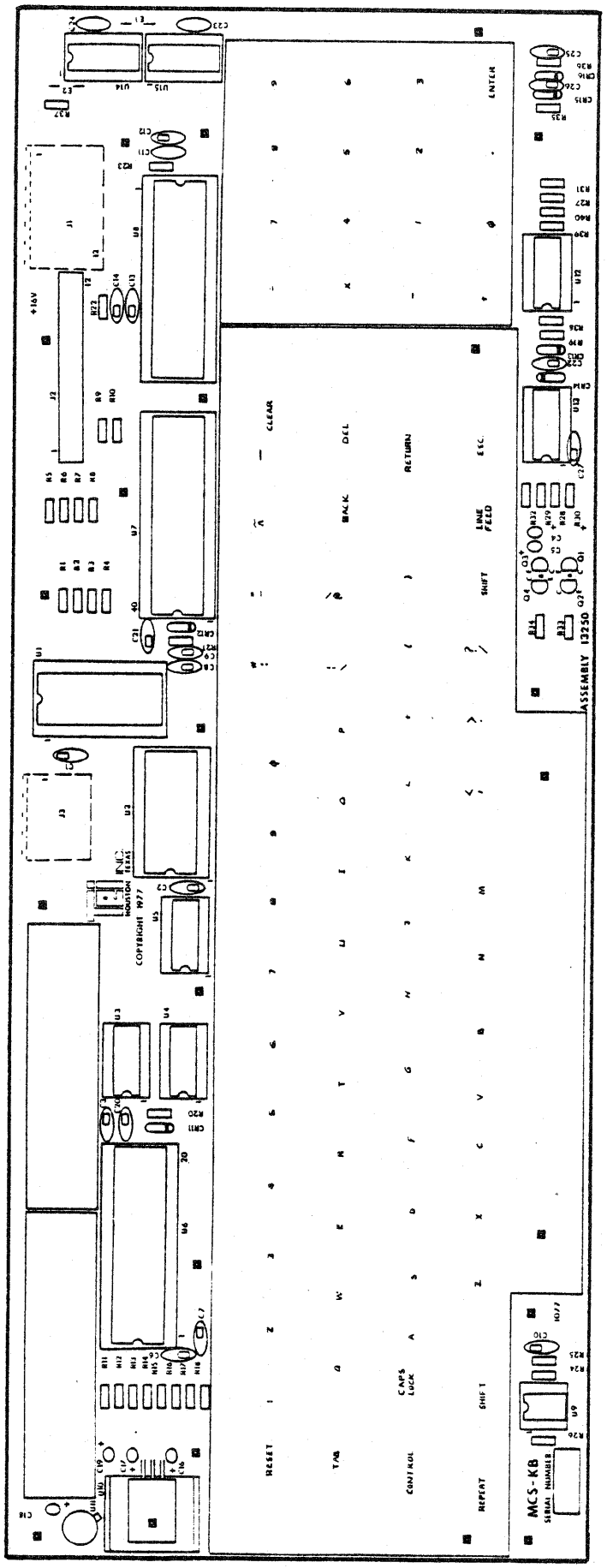
LED Board

-	FAB	13271
CR1 Thru		
CR10	LED, RED	2453-002
J1	Pin Header	
	CKT12	2125-014

Last Revision: 5/1/78 (EO 968)

3.4.1

MCS-KB COMPONENT LAYOUT



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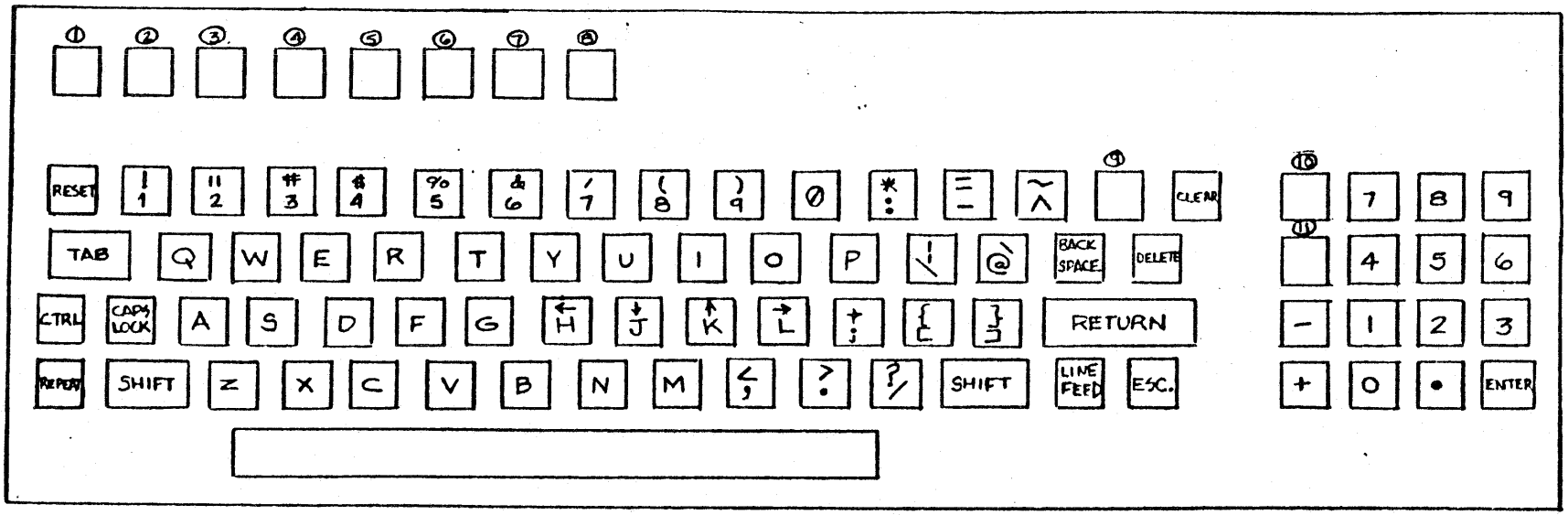


① F8
② F7
③ F6
④ F5
⑤ F4
⑥ F3
⑦ F2
⑧ F1
⑨ —
⑩ ÷
⑪ ×

NOTE: THESE CAPS TO BE ENGRAVED & FILLED IN A MODIFIED GORDON FONTE FROM A LOCAL SOURCE SO AS TO MATCH THE QUALITY LEVEL OF THE STANDARD CAP.

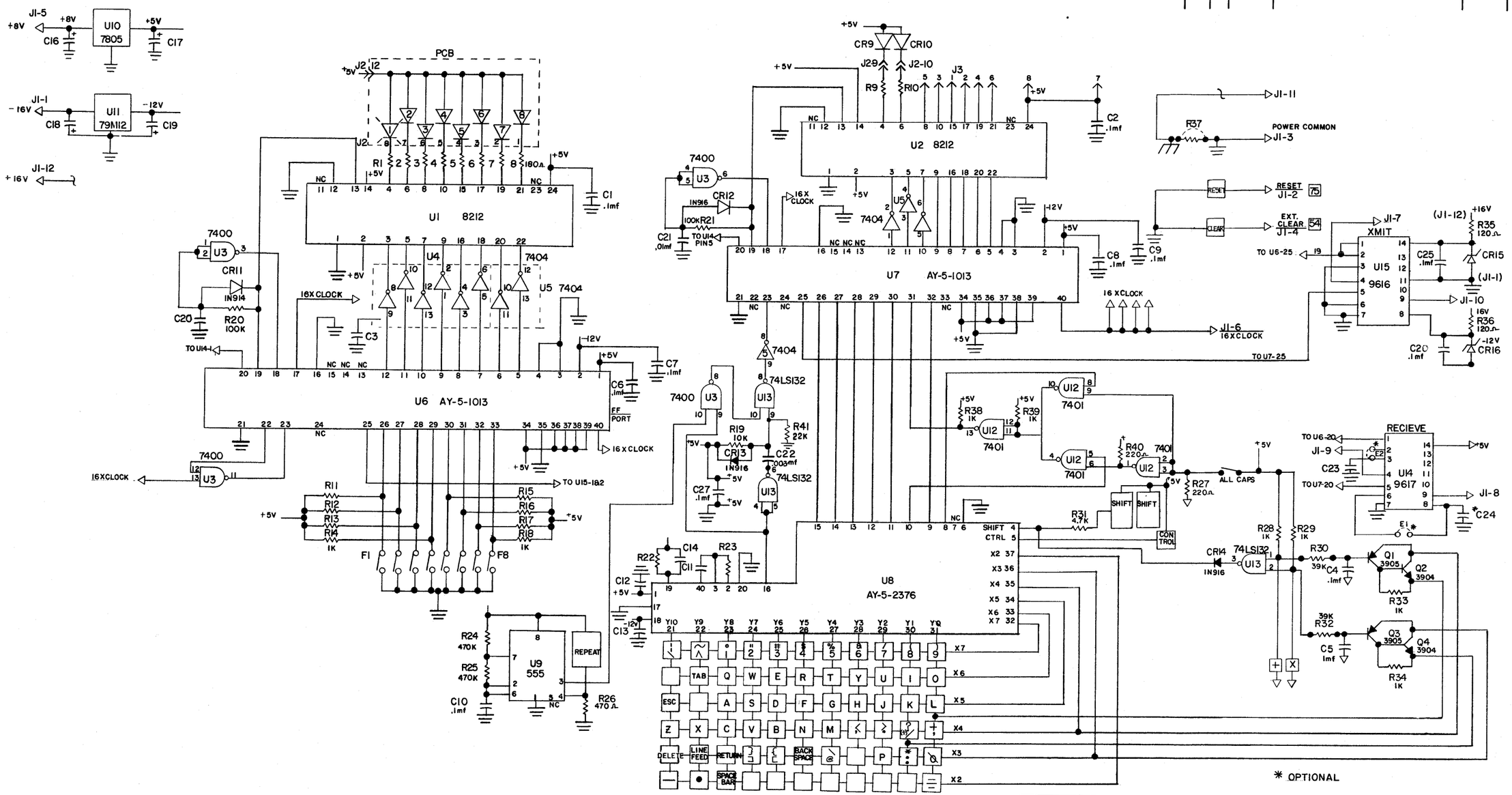
MODIFIED GORDON FONTE

TEI INC. TEXAS ELECTRONIC INSTRUMENTS, INC.	
BY CMC DATE 1/6/77	TITLE MLA KEYBOARD LAYOUT
CHK DATE	
APP	
MATL	SIZE 13324 SHT 1 OF 1

3.5 MCS-K8 INTEGRATED CIRCUIT PARTS LIST AND FUNCTION

DEVICE NO.	TYPE	LOGIC	FUNCTION
U1	8212	8 BIT LATCH	LATCH FOR BUSY-READY LED'S
U2	8212	8 BIT LATCH	LATCH FOR SPECIAL FUNCTION LED'S
U3	7400	QUAD AND	
U4	7404	HEX INVERTER	
U5	7404	HEX INVERTER	
U6	AY-5-1013	UART	SERIAL I/O FOR SPECIAL FUNCTION KEYS AND LED'S
U7	AY-5-1013	UART	SERIAL I/O FOR ASCII DATA
U8	AY-5-2376	KEYBOARD ENCODER	SEE DESCRIPTION ABOVE
U9	555	TIMER	TIMING FOR REPEAT KEY
U10	7805	5v REGULATOR	
U11	78M12	12v REGULATOR	
U12	7401	OPEN COLLECTOR AND GATES	CAPS LOCK CIRCUIT
U13	74132	SCHMIT TRIGGER AND GATES	DATA STROBE
U14	9617	TTL TO RS-232	RS-232 RECEIVER
U15	9616	TTL TO RS-232	RS-232 XMITER

REVISIONS					
ZONE	LTR	EO NO.	DESCRIPTION	DATE	APPROVED
C4	A	968	ADD R41, CHANGE R19, C22	3-13-78	



NOTES:

QTY	PART NUMBER	DESCRIPTION	MANUFACTURER	CODE IDENT	REF DES	ITEM

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.X ± .06
.XX ± .02
.XXX ± .010
ANGULAR ± .5 DEG

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

MATERIAL

CONTRACT NO.

SIGNATURES	DATE
DR D.N.C.Clarney	1-4-78
DES	
CHK Manner	4-4-78
ENGR	
APP	
APP	

TEXAS ELECTRONIC INSTRUMENTS, INC
HOUSTON, TEXAS

MCS-KB
SCHEMATIC

SIZE	CODE IDENT NO.	DWG NO.	REV
D	33179	13231	A

SCALE | REL EO NO. | SHEET 1 OF 1

DWG NO. 13231 REV

1-3-8

TEI INC.

5075 S. Loop East
Houston, Texas 77033

713-738-2300
TWX: 1-910-881-3639

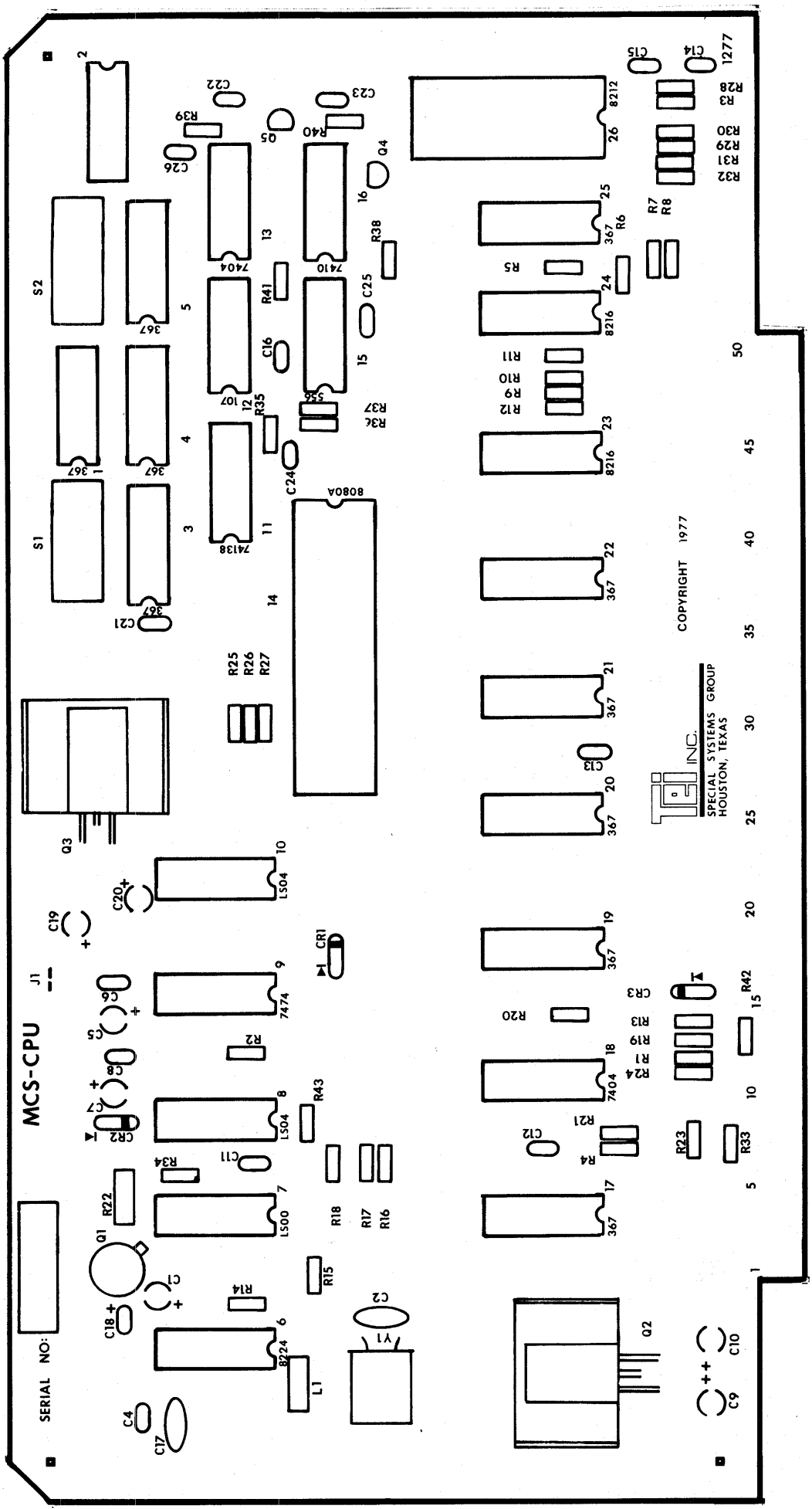
SECTION IV
MCS-CPU BOARD
TEI INC.

P/N 13686-4

SECTION IV
MSC-CPU (8080A)

		PAGE
1.	MCS-CPU COMPONENT LAYOUT	4-2
2.	PARTS LIST	4-3
3.	BUS DEFINITION CHART	4-4
4.	TEI, INC. BUS STRUCTURE DESCRIPTION	4-5
5.	SCHEMATIC DIAGRAM	4-11

MCS-CPU COMPONENT LAYOUT



TEI INC.

PARTS LIST

MCS-CPU 13328

REF DES	DESCRIPTION	TEI P/N
	PCB FAB	13281
C1,5,7,9, 10,19,20	Cap 10MF @ 20V	1580-001
C2	Cap 39PF @ 200V	1551-023
C4,6,8, 11 thru16, 18	Cap .1MF @ 50V	1562-002
C17,	Cap 47PF @ 1KV	1551-003
L1,	Choke 1.0MH	1800-001
Q1	Regulator, 78M12	3120-006
Q2,3	Regulator, 7805	3120-003
Y1,	Crystal 18.000	2300-002
Z1 thru Z5 17.19,20 thru 25	IC CHIP 74367/8T97	3161-003
Z6,	IC CHIP 8224	3162-003
Z7,	IC CHIP 74LS00	3164-002
Z8,	IC Chip 74LS02	3164-004
Z9,	IC Chip 7474	3161-020
Z10,	IC Chip 74LS04	3164-007
Z11,	IC Chip 74138	3164-009
Z12,	IC Chip 74107	3161-013
Z14,	IC Chip 8080A	3160-002
Z15,	Intergrat,CKT LM556	3100-012
Z13,18	IC Chip 7404	3161-016
Z16	IC Chip 7410	3164-006
Z23,24	IC Chip 8216	3162-002
Z26	IC Chip 8212/745412	3162-001
	Card Ejector w/pins	1700-001
CR1,	Diode IN916	4825-009
CR2,	Diode IN751A	4840-004
Q4,5	Transistor 2N3904	4864-005
R1 thru 13 R15 thru 17 R19 thru 21	1K 1/4W 2%	4741-337
R14 thru 18 R25 thru 32	5.1K 1/4W 2%	4741-405
R22	Res 470Ω 1/2W 10%	4725-306
R24,42	910Ω 1/4W 2%	4741-333
R33,J1	20 GA. Buss wire	6009-003
R36	10MΩ 1/4W 10%	4741-721
R37	4.7MΩ 1/4W 10%	4741-690
R39	39K 1/4W 2%	4741-490
R40	10K 1/4W 2%	4741-433
R41	100K 1/4W 2%	4741-529
R43	100Ω 1/4W 2%	4741-241

BUS DEFINITION:

PIN	FUNCTION
1	+8v
2	+16v
3	XRDY
4	VIØ
5	VI1
6	VI2
7	VI3
8	VI4
9	VI5
10	VI6
11	VI7
12	
13	
14	
15	
16	
17	
18	$\overline{\text{STATUS DSBL}}$
19	$\overline{\text{CCDSBL}}$
20	**
21	SS
22	$\overline{\text{ADDR DSBL}}$
23	$\overline{\text{DO DSBL}}$
24	Ø2
25	Ø1
26	PHLDA
27	PWAIT
28	PINTE
29	A 5
30	A 4
31	A 3
32	A 15
33	A 12
34	A 9
35	DO 1
36	DO Ø
37	A 10
38	DO 4
39	DO 5
40	DO 6
41	DI 2
42	DI 3
43	DI 7
44	SMI
45	SOUT
46	SINP
47	SMEMR
48	SHLTA
49	$\overline{\text{CLOCK(2 MHz)}}$
50	GND

PIN	FUNCTION
51	+8v
52	-16v
53	$\overline{\text{SSW DSB}}$
54	$\overline{\text{EXT CLR}}$
55	*
56	
57	
58	
59	
60	
61	
62	
63	
64	
65	
66	
67	$\overline{\text{PHANTOM}}$
68	MWRITE
69	****
70	***
71	RUN
72	PRDY
73	$\overline{\text{PINT}}$
74	$\overline{\text{PHOLD}}$
75	$\overline{\text{PRESET}}$
76	PSYNC
77	$\overline{\text{PWR}}$
78	PDBIN
79	A Ø
80	A 1
81	A 2
82	A 6
83	A 7
84	A 8
85	A 13
86	A 14
87	A 11
88	DO 2
89	DO 3
90	DO 7
91	DI 4
92	DI 5
93	DI 6
94	DI 1
95	DI Ø
96	SINTA
97	SWO
98	SSTACK
99	$\overline{\text{POC}}$
100	GND

* reserved for chassis ground
** reserved for memory unprotect
*** reserved for memory protect
**** reserved for protect status

TEI, INC. BUS STRUCTURE

The TEI, Inc. Bus Structure consists of 100 lines. These are arranged 50 on each side of the plug-in boards, with pins 1 through 50 on the component side and pins 51 through 100 on the back side. As the board is viewes right-side up (components up, 100 pin connector towards you) pin #1 is on the left end on the top and pin 51 is on the back side directly opposite pin #1.

Conventions:

SYMBOLS: "P" prefix indicates a processor command or control signal

"S" prefix indicates a processor status signal

LOADING: All inputs to a card should be loaded with a maximum of 1 TTL low power load

LEVELS: All bus signals except the power supply are TTL. All Data and Address lines are positive TRUE (ground = 0 bit)

BUS DEFINITION

Front Side

No.	SYMBOL	NAME	FUNCTION
1	+8V	+8 volts	Unregulated input to 5v regulators
2	+16V	+16 volts	Positive unregulated voltage
3	XRDY	External Ready	Used by Front Panel: Pulling this line low will cause the processor to enter a WAIT state and allows the status of the normal Ready Line (PRDY) to be examined.
4	V10	Vectored Interrupt Line #0	
5	V11	Vectored Interrupt Line #1	
6	V12	Vectored Interrupt Line #2	
7	V13	Vectored Interrupt Line #3	
8	V14	Vectored Interrupt Line #4	
9	V15	Vectored Interrupt Line #5	

BUS DEFINITION

FRONT SIDE

No.	SYMBOL	NAME	FUNCTION
10	V16	Vectored Interrupt Line #6	
11	V17	Vectored Interrupt Line #7	
12 to 17	UNUSED		
18	$\overline{\text{STATUS DSBL}}$	STATUS DISABLE	Allows the buffers for the 8 status lines to be tri-stated
19	$\overline{\text{CC DSB}}$	COMMAND CONTROL DISABLE	Allows the buffers for the 6 output command/control lines to be tri-stated
20	UNPROT	UNPROTECT	Reserved for input to the memory protect flip-flop on a given memory board
21	SS	SINGLE STEP	Used by Front Panel to disable input buffer while panel drives bidirectional data bus
22	$\overline{\text{ADDR DSBL}}$	ADDRESS DISABLE	Allows the buffers for the 16 address lines to be tri-stated
23	$\overline{\text{DO DSBL}}$	DATA OUT DISABLE	Allows the bidirectional data bus drivers for the 8 data lines to be tri-stated for both input and output data buses
24	Ø2	Phase 2 Clock	
25	Ø1	Phase 1 Clock	
26	PHLDA	Hold Acknowledge	Processor control output signal which appears in response to the HOLD signal; indicates that the data and address bus will go to the high impedance state on the 8080. Note: ADDR DSBL and DO DSBL must be driven to tri-state the system bus.

BUS DEFINITION

FRONT SIDE

No.	SYMBOL	NAME	FUNCTION
27	PWAIT	WAIT	Processor control output signal which acknowledges that the processor is in a WAIT state
28	PINTE	INTERRUPT ENABLE	Processor control output signal indicating interrupts are enabled: may be set or reset by E1 and D1 instruction and inhibits interrupts from being accepted by the CPU if it is reset
29	A5	Address Line #5	
30	A4	Address Line #4	
31	A3	Address Line #3	
32	A15	Address Line #15	
33	A12	Address Line #12	
34	A9	Address Line #9	
35	DØ1	Data Out Line #1	
36	DO0	Data Out Line #0	
37	A10	Address Line #10	
38	DO4	Data Out Line #4	
39	DO5	Data Out Line #5	
40	DO6	Data Out Line #6	
41	DI2	Data In Line #2	
42	DI3	Data In Line #3	
43	DI7	Data In Line #7	
44	SM1	M1	Status output signal that indicates that the processor is in the fetch cycle for the first byte of an instruction

BUS DEFINITION

Front Side

NO.	SYMBOL	NAME	FUNCTION
45	SOUT	OUT	Status output signal which indicates that the address bus contains the address of an output device and the data bus will contain the output data when PWR is active
46	SNIP	INP	Status output signal which indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when PDBIN is active
47	SMEMR	MEMR	Status output signal which indicates that the data bus will be used for memory read data
48	SHLTA	HLTA	Status output signal which acknowledges a HALT instruction
49	$\overline{\text{CLOCK}}$	CLOCK	2 MHz clock signal
50	GND	GROUND	

Back Side

No.	SYMBOL	NAME	FUNCTION
51	+8V	+8 volts	Unregulated input to 5v regulators
52	-16V	-16 volts	Negative unregulated voltage
53	$\overline{\text{SSW DSB}}$	SENSE SWITCH DISABLE	Disables the data input buffers so the input from the sense switches may be strobed onto the bidirectional data bus
54	$\overline{\text{EXT CLR}}$	EXTERNAL CLEAR	Clear signal for I/O devices (front panel switch closure to ground)
55	CGND	CHASSIS GROUND	
56 to 66	NOT USED		
67	$\overline{\text{PHANTOM}}$	PHANTOM DISABLE	Used to disable RAM or ROM during power on initialization program execution

BUS DEFINITION

BACK SIDE

No.	SYMBOL	NAME	FUNCTION
68	MWRT	MEMORY WRITE	From the Front Panel indicates that the current data on the Data Out Bus is to be written into the memory location currently on the address bus
69	$\overline{PS}$	PROTECT STATUS	Reserved to indicate the status of the memory protect flip-flop on the memory board currently addressed
70	PROT	PROTECT	Reserved for input to the memory protect flip-flop on the memory board currently addressed
71	RUN	RUN	Indicates that the RUN/STOP flip-flop is set to run on the front panel
72	PRDY	READY	Processor command/control input that controls the run state of the processor; if the line is pulled low the processor will enter a wait state until the line is released
73	$\overline{PINT}$	INTERRUPT REQUEST	The processor recognizes an interrupt request on this line at the end of the current instruction or while halted. If the processor is in the HOLD state or the Interrupt Enable flip-flop is reset, it will not honor the request
74	$\overline{PHOLD}$	HOLD	Processor command input signal which requests the processor to enter the HOLD state; allows an external device to gain control of address and data buses as soon as the processor has completed its use of these buses for the current machine cycle
75	$\overline{PRESET}$	RESET	Processor command input; while activated the content of the program counter is cleared and the instruction register is set to 0
76	PSYNC	SYNC	Processor control output provides a signal to indicate the beginning of each machine cycle
77	$\overline{PWR}$	WRITE	Processor control output used for memory write or I/O output control; data on the data bus is stable while the $\overline{PWR}$ is active

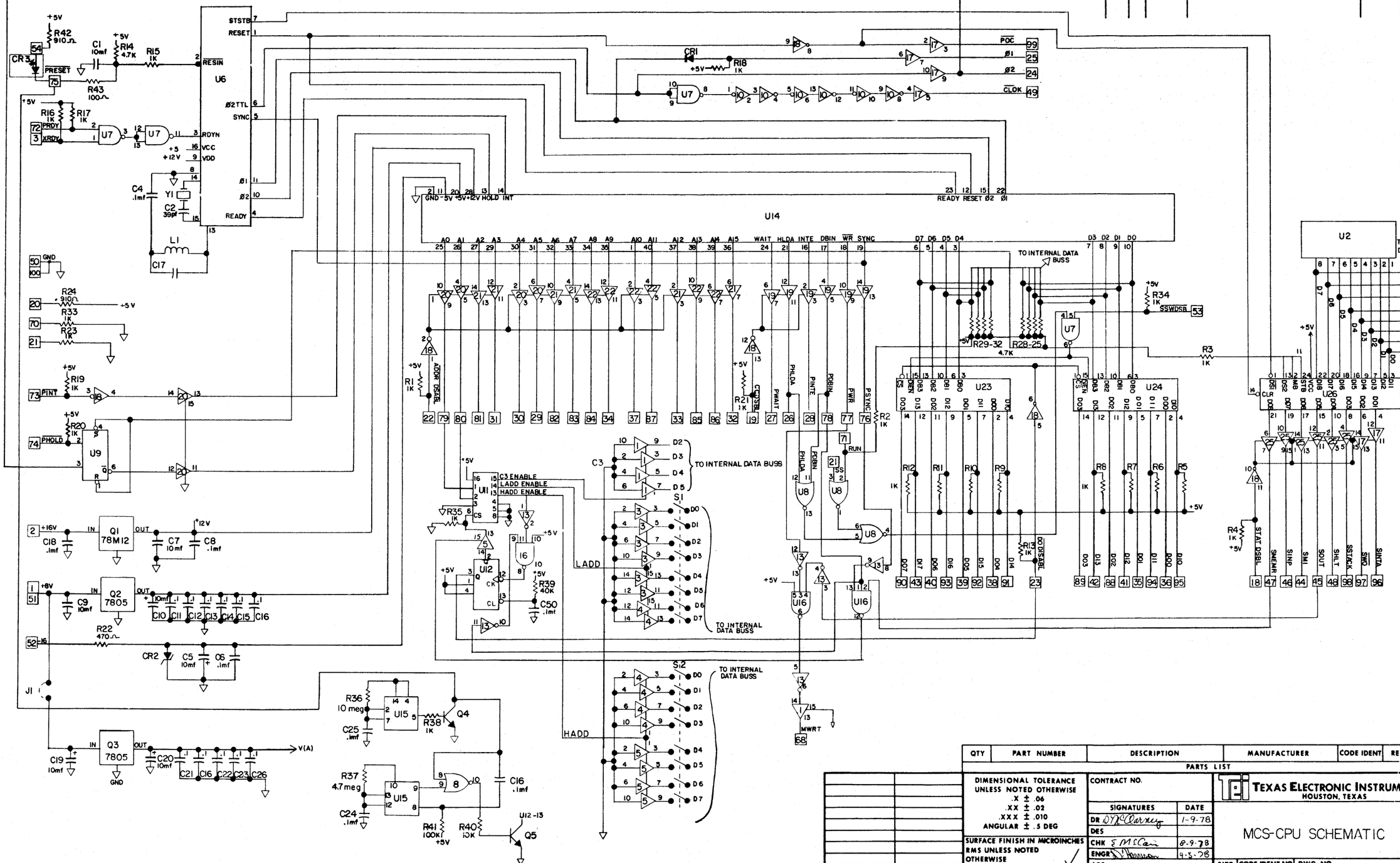
BUS DEFINITION

Back Side

No.	SYMBOL	NAME	FUNCTION
78	PDBIN	DATA BUS IN	Processor control output signal indicates to external circuits that the data bus is in the input mode
79	A0	Address Line #0	
80	A1	Address Line #1	
81	A2	Address Line #2	
82	A6	Address Line #6	
83	A7	Address Line #7	
84	A8	Address Line #8	
85	A13	Address Line #13	
86	A14	Address Line #14	
87	A11	Address Line #11	
88	DO2	Data Out Line #2	
89	DO3	Data Out Line #3	
90	DO7	Data Out Line #7	
91	DI4	Data In Line #4	
92	DI5	Data In Line #5	
93	DI6	Data In Line #6	
94	DI7	Data In Line #7	
95	DI0	Data In Line #0	
96	SINTA	INTA	Status output signal to acknowledge signal for INTERRUPT request
97	SWO	WO	Status output signal indicates that the operation in the current machine cycle will be a WRITE memory or output function
98	SSTACK	STACK	Status output signal indicates that the address bus holds the pushdown stack address from the Stack Pointer
99	$\overline{\text{POC}}$	Power-on Clear	
100	GND	GROUND	

REVISIONS					
ZONE	LTR	EO NO.	DESCRIPTION	DATE	APPROVED
	A	1034	UPDATED COMPONENT MARKING	8-9-78	EMS

*Optional



NOTES:

QTY	PART NUMBER	DESCRIPTION	MANUFACTURER	CODE IDENT	REF DES	ITEM

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.X ± .06
.XX ± .02
.XXX ± .010
ANGULAR ± .5 DEG

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

MATERIAL

CONTRACT NO.

SIGNATURES	DATE
DR D.P. McCarney	1-9-78
DES	
CHK S. McCain	8-9-78
ENGR	9-5-78
APP	
APP	

TEXAS ELECTRONIC INSTRUMENTS, INC
HOUSTON, TEXAS

MCS-CPU SCHEMATIC

SIZE	CODE IDENT NO.	DWG NO.	REV
D	33179	13225	A
SCALE	REL EO NO.	SHEET 1 OF 1	

14-11

TEI INC.

5075 S. Loop East
Houston, Texas 77033

713-738-2300
TWX: 1-910-881-3639

SECTION V
3P + 3S I/O PC BOARD
TEI INC.

P/N 13686-5

SECTION V

MCS-I/O 3P + 3S

1. BASIC DESCRIPTION 5-3
2. I.C. LIST & FUNCTION 5-4
3. INPUT/OUTPUT CABLES/CONNECTORS
   - A. SERIAL PORT 5-6
   - B. PARALLEL CABLE 5-7
4. MCS-I/O 3P + 3S COMPONENT LAYOUT 5-8
5. PARTS LIST 5-9
6. COMPONENT SPECIFICATIONS
   - 8251 USART 5-11
   - 8255A PROGRAMMABLE INTERFACE 5-12
   - AY-5-1013 UARK 5-13
   - 7493 4-BIT BINARY COUNTER 5-15
   - µA9616 TRIPLE LINE DRIVER 5-16
   - µA9617 TRIPLE LINE RECEIVER 5-17
7. SCHEMATIC DIAGRAM 5-19

TEI, INC. 3P+3S I/O CARD

BASIC DESCRIPTION OF INPUT/OUTPUT

THIS CARD CONTAINS 3 SERIAL PORTS FOR INPUT & OUTPUT. TWO ARE ASYNCHRONOUS AND ONE PROGRAMMABLE AS SYNCHRONOUS OR ASYNCHRONOUS. IN ADDITION 24 BITS OF PARALLEL I/O ARE AVAILABLE.

UART (A): (AY 5-1013 U-10)
THIS SERIAL PORT COMES FACTORY SET TO PORT FF (HEX)-DATA
FE (HEX)-STATUS

8 CHARACTER BITS
2 STOP BITS (SYSTEM USE--FUNCTION KEYS AND BIT LIGHTS ON KEYBOARD)
EVEN PARITY

PORT ADDRESSING MAY BE CHANGED BETWEEN F8(HEX) THRU FF(HEX)
THE NUMBER OF CHARACTER BITS/STOP BITS/AND PARITY IS JUMPER OPTIONAL ALSO.

UART (B): (AY 5-1013 U-17)
THIS SERIAL PORT COMES FACTORY SET TO PORT 01(HEX)-DATA
00(HEX)-STATUS

7 CHARACTER BITS
2 STOP BITS (SYSTEM USE--KEYBOARD AND READY/BUSY LIGHTS)
EVEN PARITY

UART PORT ADDRESSING MAY BE CHANGED WITHIN 1 OF 16 PORTS SHARED BY 2 OTHER CHIPS (THE USART AND 8255A). THE 16 PORT BLOCK MAY BE MOVED WITHIN ANY 16 PORT BLOCK OUT OF THE 256 I/O PORT ADDRESSES. THE NUMBER OF CHARACTER BITS , STOP BITS , AND ODD OR EVEN PARITY ARE JUMPER SELECTABLE.

USART : (8251 U-3)
THIS IS A PROGRAMMABLE SERIAL INPUT/OUTPUT DEVICE

THIS SERIAL PORT COMES FACTORY SET TO PORT 02(HEX)-DATA
03(HEX)-STATUS

CHARACTER BITS, STOP BITS, PARITY, (SYSTEM USE--PRIMARILY ASSIGNED AS OPTIONAL RS 232 I/O FOR SERIAL PRINTER) AND OTHER FUNCTIONS ARE SOFTWARE PROGRAMMABLE.

.....

ALL 3 OF THE ABOVE SERIAL DEVICES HAVE TTL AND RS-232 DATA SIGNAL LEVELS FOR INTERFACING AVAILABLE AT THE I/O CARD CONNECTOR. ALL OTHER SERIAL (HANDSHAKING) SIGNAL'S ARE TTL ONLY.

.....

PARALLEL DEVICE: (8255A U-4)
THE 24 BIT I/O DEVICE OCCUPIES 4 PORT ADDRESSES AND
COMES FACTORY SET TO THE FOLLOWING PORTS:

8255	PORT A	04(HEX) DATA
	PORT B	05(HEX) SYSTEM USE--PARALLEL PRINTER OUTPUT)
	PORT C	06(HEX) HAND SHAKING (STROBE, BUSY ...)
		07(HEX) COMMAND/CONTROL

* REFER TO 8255A DATA SHEET FOR DETAILS OF OPERATION.

THIS CARD IS DESIGNED TO OPERATE WITH A 2Mhz CLOCK PROVIDED FROM THE S100 BUSS.
BAUD RATES ARE JUMPER SELECTABLE FOR 75 THRU 19,200 BAUD.

TO OPTION THE I/O CARD FOR SPECIAL PURPOSES, REFER TO I/O CARD OPTION TABLE.

****

DEVICE NO.	CHIP	TYPE	LOGIC FUNCTION
U1	9616	RS-232	DRIVER INTERNAL SLEW RATE LIMITING MEETS EIA RS-232-C AND CCITT V.24 SPECIFICATIONS SUPPLY INDEPENDENT OUTPUT SWING OUTPUT CURRENT LIMITING
U2	9617	RS-232	RECEIVER MEETS ALL EIA RS-232-C AND CCITT V.24 SPECIFICATIONS FAIL-SAFE OPERATION INDIVIDUAL RESPONSE CONTROLS
U3	8251	USART	PROGRAMMABLE COMMUNICATION INTERFACE (SERIAL DATA) SYNCHRONOUS AND ASYNCHRONOUS OPERATION SYNCHRONOUS: 5-8 BIT CHARACTERS INTERNAL OR EXTERNAL CHARACTER SYNCHRONIZATION AUTOMATIC SYNC INSERTION ASYNCHRONOUS: 5-8 BIT CHARACTERS PROGRAMMABLE CLOCK RATE-1, 16 or 64 TIMES BAUD RATE BREAK CHARACTER GENERATION 1, 1 1/2, OR 2 STOP BITS FALSE START BIT DETECTION FULL DUPLEX, DOUBLE BUFFERED, TRANSMITTER AND RECEIVER ERROR DETECTION--PARITY, OVERRUN, AND FRAMING
U4	8255A	PROGRAMMABLE PERIPHERAL INTERFACE	(PARALLEL - 3 EIGHT BIT PORTS) 24 PROGRAMMABLE I/O PINS DIRECT BIT/RESET CAPABILITY INTERRUPT CONTROL CAPABILITY

U5, U11, U12, AND U18	7493	4-BIT BINARY COUNTER (BAUD RATE)
U6	7421	DUAL 4-INPUT AND GATE (PORT ADDRESSES DECODE CIRCUIT)
U7	7400	QUAD 2-INPUT NAND GATE (PORT ADDRESS DECODE CIRCUIT) (1/2 OF THIS CHIP IS UN-USED)
U8	74368	TRI-STATEABLE LINE DRIVER (DECODE AND UART STATUS)
U9	7402	QUAD 2-INPUT NOR GATE (UART/USART-READ/WRITE LOGIC)
U10	AY-5-1013A	UART (A) SYSTEM KEYBOARD
U13	74154	ONE OF SIXTEEN DECODER (PORT DECODE CHIP)
U14	7410	3-INPUT NAND GATE (READ/WRITE LOGIC
U15	7400	QUAD 2-INPUT NAND GATE (READ/WRITE LOGIC)
U16	74368	TRI-STATEABLE LINE DRIVER (READ/WRITE-UART STATUS)
U17	AY-5-1013A	UART (B) (SYSTEM KEYBOARD (8) BIT LIGHTS)
U19	7430	8-INPUT NAND GATE (PORT F8-FF(HEX) DECODE CIRCUIT)
U20	7404	HEX INVERTER (ADDRESS BIT INVERSION (PORT BITS))
U21	74138	ONE OF EIGHT DECODER (PORT F8-FF (HEX))
U22 & U23	8216	4 BIT PARALLEL BIDIRECTIONAL BUS DRIVER (DATA BUFFERS INPUT/OUTPUT SYSTEM BUS

POWER REGULATION:

+5VDC POWER FOR TTL Vcc 2 7805 ON CARD REGULATORS WITH HEATSINK'S
+12VDC POWER FOR 9616 RS-232 DRIVER (ONLY +12VDC REQUIRED) ZENER DIODE IN759A
-12VDC POWER FOR UARTS, AND 9616 RS-232 DRIVER ZENER DIODE IN759A

SERIAL PORTS:
CONNECTOR J3 (34 PIN RIBBON CABLE) SIGNALS ARE AS FOLLOWS

PIN #	FUNCTION
1	UART B XMIT (TTL)
2	UART B RECV (TTL)
3	UART B XMIT (RS-232-C)
4	UART B RECV (RS-232-C)
5	SYSTEM HARDWARE RESET FROM KEYBOARD
6	EXT CLR SYSTEM KEYBOARD SIGNAL (NEG. TRUE)
7	UART CLOCK (CAN RECEIVE OR TRANSMIT CLOCK)
8	+8VDC UN-REGULATED RAW POWER (SYSTEM KEYBOARD)
9	+16VDC UN-REGULATED RAW POWER (SYSTEM KEYBOARD)
10	-16VDC UN-REGULATED RAW POWER (SYSTEM KEYBOARD)
11	GROUND (POWER AND SIGNALS)
12	UART A XMIT (TTL)
13	UART A RECV (TTL)
14	UART A XMIT (RS-232-C)
15	UART A RECV (RS-232-C)
16	GROUND (SIGNAL)
17	+8VDC UN-REGULATED RAW POWER
18	+16VDC UN-REGULATED RAW POWER
19	-16VDC UN-REGULATED RAW POWER
20	GROUND (POWER)
21	SNYC DET. OUTPUT (USART SIGNAL (SYNCHRONOUS MODE))
22	RECIEVER READY (USART)
23	XMIT EMPTY (USART)
24	DATA TERMINAL READY (USART) (NEG. TRUE)
25	CLEAR TO SEND (USART) (NEG. TRUE)
26	DATA SET READY (USART) (NEG. TRUE)
27	REQUEST TO SEND (USART) (NEG. TRUE)
28	DATA TERMINAL READY (USART) (NEG. TRUE)
29	USART CLOCK (BAUD RATE CLOCK GEN.) (CAN RECEIVE OR TRANSMIT CLOCK)
30	GROUND (SIGNAL)
31	USART XMIT (RS-232-C)
32	USART RECV (RS-232-C)
33	USART XMIT (TTL)
34	USART RECV (TTL)

NOTE: JUMPERS "VS" MUST BE JUMPERED TO +8, +16, AND -16 TO HAVE POWER (RAW) EXIT THROUGH CABLE J3 THESE JUMPERS ARE TO KEEP RAW D. C. POWER OUT OF CABLE IF NOT NEEDED. THESE 3 JUMPERS ARE SHIPPED CONNECTED FOR KEYBOARD POWER. SINCE POWER IS AVAILABLE AT THIS CONNECTOR, EXTREME CAUTION SHOULD BE USED IN WIRING UP CABLES TO THIS CONNECTOR. IF POWER IS NOT NEEDED FROM THIS SOURCE, CUT THE JUMPERS ON THE CARD TO REMOVE POWER FROM THE CONNECTOR. IF USED, THE POWER IS NOT FUSED ON THE CARD, AND ANY PROTECTION FROM OVERLOAD MUST BE INHERENT IN THE MOTHERBOARD POWER SOURCE AND/OR PRE-CAUTIONARY STEPS MUST BE APPLIED IN THE PERIPHERAL THAT USES THIS POWER. COMBINED CURRENT AVAILABLE FOR PERIPHERALS SHOULD NOT EXCEED TH' FOLLOWING:

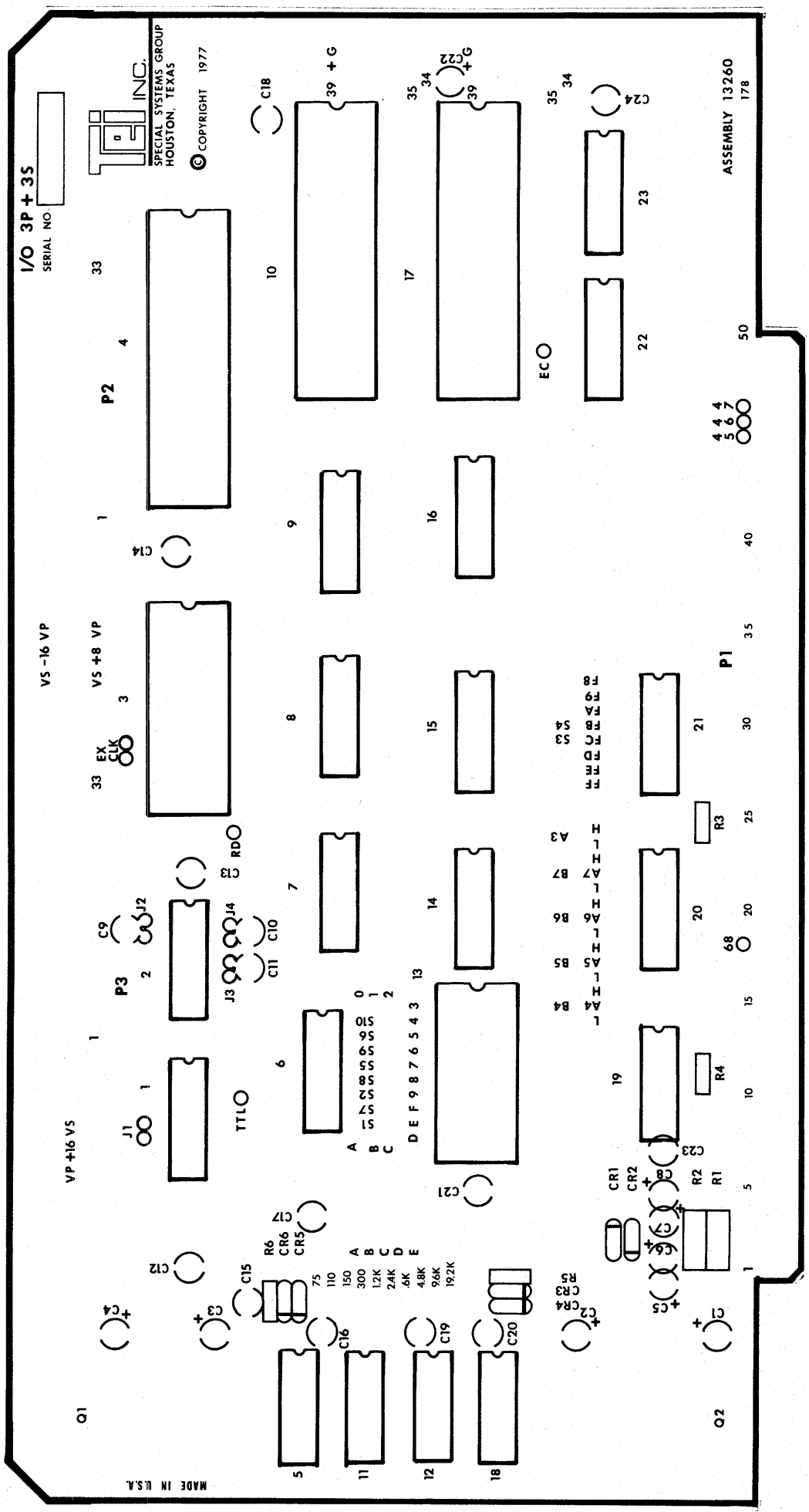
+8V	+16V	-16V
200MA	100MA	100MA

PARALLEL CABLE (CONNECTOR J2)

1	PORT B BIT 0
2	PORT B BIT 1
3	PORT B BIT 2
4	PORT B BIT 3
5	PORT B BIT 4
6	PORT B BIT 5
7	PORT B BIT 6
8	PORT B BIT 7
9	PORT C BIT 0
10	PORT C BIT 1
11	PORT C BIT 2
12	PORT C BIT 3
13	GROUND (SIGNAL)
14	+8 VDC RAW UN-REGULATED POWER (EXT. CIRCUITRY)
15	-16 VDC RAW UN-REGULATED POWER (EXT. CIRCUITRY)
16	+16 VDC RAW UN-REGULATED POWER (EXT. CIRCUITRY)
17	GROUND (POWER)
----------SPLIT CABLE HERE FOR CUAL 12 BIT PORT CONTROL----------	
18	+16 VDC RAW UN-REGULATED POWER (EXT. CIRCUITRY)
19	-16 VDC RAW UN-REGULATED POWER (EXT. CIRCUITRY)
20	+8 VDC RAW UN-REGULATED POWER (EXT. CIRCUITRY)
21	GROUND (POWER)
22	PORT C BIT 4
23	PORT C BIT 5
24	PORT C BIT 6
25	PORT C BIT 7
26	GROUND (SIGNAL)
27	PORT A BIT 0
28	PORT A BIT 1
29	PORT A BIT 2
30	PORT A BIT 3
31	PORT A BIT 4
32	PORT A BIT 5
33	PORT A BIT 6
34	PORT A BIT 7

NOTE: JUMPER "VP" MUST BE CONNECTED TO +8, +16, AND -16 IN ORDER TO MAKE POWER AVAILABLE AT CONNECTOR J2. ALL THE PRECAUTIONS COVERING RAW POWER FOR THE SERIAL CONNECTOR.

MCS- I/O 3P+3S COMPONENT LAYOUT



TEI INC.

PARTS LIST

MCS-3P+3S I/O Board

REF DES	DESCRIPTION	TEI P/N
C1, C2, C3, C4, C5, C6, C7, C8	Cap 10 uf @ 20V	1580-001
C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24	Cap, .1 uf	1562-002
CR1, CR2	Diode IN759A	4840-011
CR3, CR4, CR5, CR6	Diode IN916	4825-009
Q1, Q2	Regulator 7805	3120-003
R1	150 Ω 1/2 W 10% RES	4725-258
R2	120 Ω 1/2 W 10% RES *	4725-249
R3, R4, R5, R6	RES. 4.7K 1/4 W 2%	4741-402
U1	IC Chip 9616	3160-009
U2	IC Chip 9617	3160-010
U3	IC Chip 8251	3162-005
U4	IC Chip 8255	3162-006
U5, U11, U12, U18	IC Chip 7493	3161-012
U6	IC Chip 7421	3161-014
U8, U16	IC Chip 74368	3161-010
U9	IC Chip 7402	3161-019
U10, U17	IC Chip AY5-1013	3100-013
U13	IC Chip 74LS154	3164-008
U14	IC Chip 7410	3161-034
U15, U7	IC Chip 7400	3161-018
U19	IC Chip 7430	3161-032
U20	IC Chip 7404	3161-016
U21	IC Chip 74LS138	3164-009
U22, U23	IC Chip 8216	3162-002
P2, P3	Connector, 34 Pin	2125-012
-	Card Ejector	1700-001

* 100Ω may be used for R2.

REF DES	DESCRIPTION	TEI P/N

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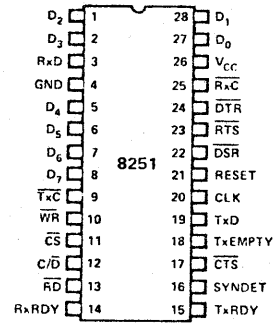
intel

8251
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
  - **Synchronous:**
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
  - **Asynchronous:**
    - 5-8 Bit Characters
    - Clock Rate — 1, 16 or 64 Times Baud Rate
    - Break Character Generation
    - 1, 1½, or 2 Stop Bits
    - False Start Bit Detection
- **Baud Rate —DC to 56k Baud (Sync Mode)**
  DC to 9.6k Baud (Async Mode)
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun, and Framing**
- **Fully Compatible with 8080 CPU**
- **28-Pin DIP Package**
- **All Inputs and Outputs Are TTL Compatible**
- **Single 5 Volt Supply**
- **Single TTL Clock**

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) Chip designed for data communications in microcomputer systems. The USART is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPT. The chip is constructed using N-channel silicon gate technology.

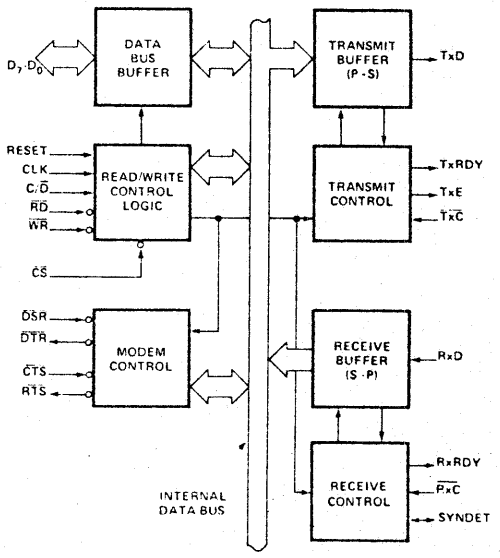
PIN CONFIGURATION



Pin Name	Pin Function
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

Pin Name	Pin Function
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
Vcc	+5 Volt Supply
GND	Ground

BLOCK DIAGRAM



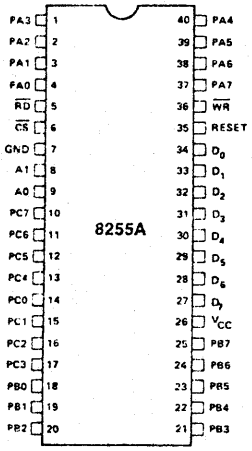
8255A
PROGRAMMABLE PERIPHERAL INTERFACE

- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with MCS-80™ Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40 Pin Dual-In-Line Package
- Reduces System Package Count
- Improved DC Driving Capability

The 8255A is a general purpose programmable I/O device designed for use with both the 8008 and 8080 microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a Bi-directional Bus mode which uses 8 lines for a bi-directional bus, and five lines, borrowing one from the other group, for handshaking.

Other features of the 8255A include bit set and reset capability and the ability to source 1 mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.

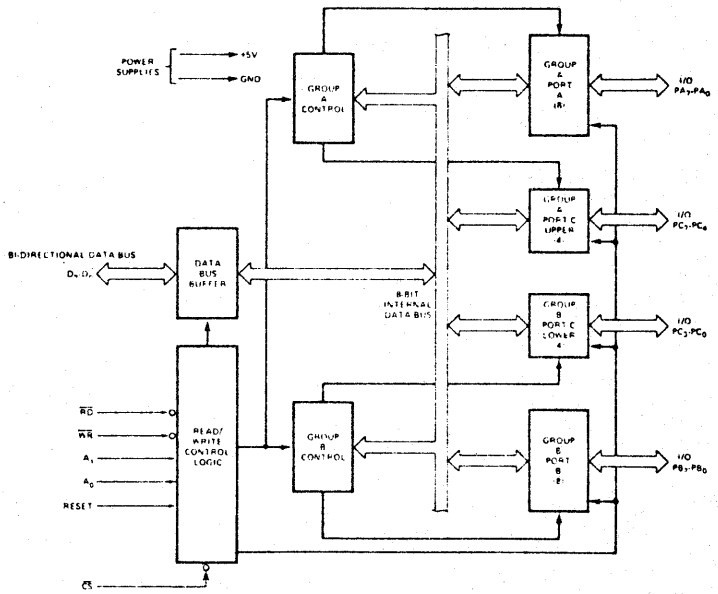
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255A BLOCK DIAGRAM



UAR/T Universal Asynchronous Receiver/Transmitter

FEATURES

- DTL and TLL compatible—no interfacing circuits required—drives one TTL load.
- Fully Double Buffered—eliminates need for system synchronization, facilitates high-speed operation.
- Full Duplex Operation—can handle multiple baud rates (receiving-transmitting) simultaneously.
- Start Bit Verification—decreases error rate with center sampling.
- Receiver center sampling of serial input; 46% distortion immunity.
- High Speed Operation.
- Three-State Outputs—bus structure capability.
- Low Power-minimum power requirements.
- Input Protected—eliminates handling problems.

AY-5-1013/1013A
- GIANT P-channel nitride process.
- 0 to 30kbaud/0 to 40kbaud.
- Pull up resistors to V_{CC} on all inputs.

AY-6-1013
- GIANT P-channel nitride process.
- 0 to 20kbaud.
- Extended Operating Temperature Range:
  -40° C to +85° C (plastic package)
  -55° C to +125° C (ceramic package)
- Pull-up resistors to V_{CC} on all inputs.

AY-3-1014A/1015
- Single Supply Operation:
  +4.75V to +14V (AY-3-1014A)
  +4.75V to +5.25V (AY-3-1015)
- CMOS compatible (AY-3-1014A).
- 1½ stop bit mode.
- External reset of all registers.
- GIANT II N-channel Ion Implant Process.
- 0 to 30kbaud.
- Pull-up resistors to V_{CC} on all inputs (AY-3-1015).

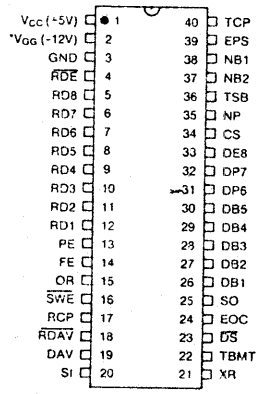
DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits (1½ stop bit capability with the AY-3-1014A/1015), and either odd/even parity or no parity. In order to make the UAR/T universal, the baud, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL/CMOS logic without the need for interfacing components. All strobed outputs are three-state logic.

PIN CONFIGURATION

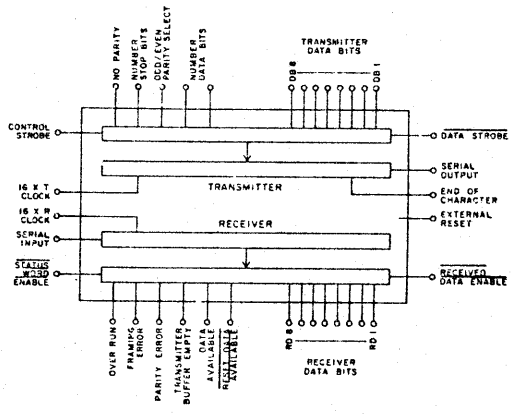
40 LEAD DUAL IN LINE

Top View



*Pin 2: AY-3-1014A/1015 — No Connection.

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
1	V_{CC} Power Supply (V_{CC})	+5V Supply
2	V_{GG} Power Supply (V_{GG})	−12V Supply (Not connected for AY-3- 1014A/1015)
3	Ground (V_{SS})	Ground
4	Received Data Enable ($\overline{RDE}$)	A logic "O" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits (RD8-RD1)	These are the 8 data output lines. Received characters are right justified: the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL ouput characteristics when $\overline{RDE}$ is "O" and a high impedance state when $\overline{RDE}$ is "1". Thus, the data output lines can be bus structure oriented.
13	Parity Error (PE)	This lines goes to a logic "1" if the received character parity does not agree with the selected parity. Tri-state.
14	Framing Error (FE)	This line goes to a logic "1" if the received character has no valid stop bit. Tri-state.
15	Over-Run (OR)	This line goes to a logic "1" if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tri-state.
16	Status Word Enable ($\overline{SWE}$)	A logic "O" on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. Tri-state.
17	Receiver Clock (RCP)	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud.
18	Reset Data Available ($\overline{RDAV}$)	A logic "O" will reset the DAV line. The DAV F/F is only thing that is reset.
19	Data Available (DAV)	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register. Tri-state. Fig.12,34.
20	Serial Input (SI)	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "O") transition is required for initiation of data reception. Fig.11,12,33,34.
21	External Reset (XR)	Resets all registers (except that the received data register is not reset in the AY-5-1013/1013A and AY-6-1013). Sets SO, EOC, and TBMT to a logic "1". Resets DAV, and error flags to "O". Clears input data buffer. Must be tied to logic "O" when not in use.
22	Transmitter Buffer Empty (TBMT)	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character. Tri-state. See Fig.18,20,40,42.
23	Data Strobe ($\overline{DS}$)	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of $\overline{DS}$. Data must be stable during entire strobe.
24	End of Character (EOC)	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Fig.17,19,39,41.
25	Serial Output (SO)	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted. See Fig.16.
26-33	Data Bit Inputs (DB1-DB8)	There are up to 8 data bit input lines available.
34	Control Strobe (CS)	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	No Parity (NP)	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "O".
36	Number of Stop Bits (TSB)	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits. For the AY-3-1014A/1015, the combined selection of 2 stop bits and 5 bits/character will produce 1½ stop bits.
37-38	Number of Bits/Character (NB2, NB1)	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character. NB2 NB1 Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	Odd/Even Parity Select (EPS)	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "O" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock (TCP)	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud.

TTL/MSI 9393/5493, 7493
4-BIT BINARY COUNTER

DESCRIPTION – The TTL/MSI 9393/5493, 7493 is a 4-Bit Binary Counter consisting of four master/slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a LOW level. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output Q_A must be externally connected to input $\overline{CP}_B$. The input count pulses are applied to input $\overline{CP}_A$. Simultaneously divisions of 2, 4, 8 and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs as shown in the truth table.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input $\overline{CP}_B$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

These circuits are completely compatible with TTL and DTL logic families.

PIN NAMES

		LOADING
R_0	Reset-Zero Input	1 U.L.
$\overline{CP}_A$	Clock (Active LOW going edge) Input	2 U.L.
$\overline{CP}_B$	Clock (Active LOW going edge) Input	2 U.L.
Q_A, Q_B, Q_C, Q_D	Outputs	10 U.L.

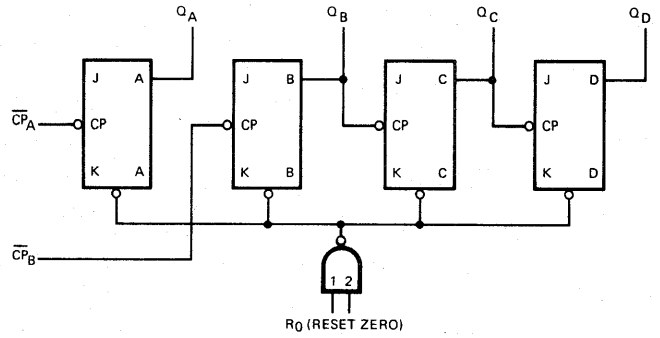
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

TRUTH TABLE (See Notes 1, 2 and 3)

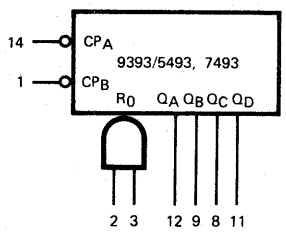
COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES:
1. Output Q_A connected to input $\overline{CP}_B$.
2. To reset all outputs to LOW level both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at HIGH level state.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a LOW level to count.

LOGIC DIAGRAM

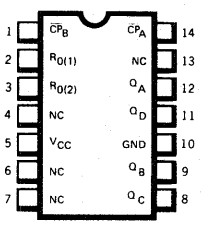


LOGIC SYMBOL

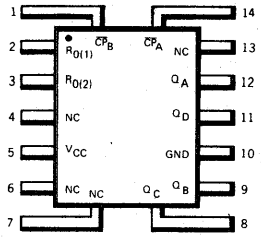


V_{CC} = Pin 5
GND = Pin 10
N.C. = Pins 4, 6, 7, 13

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



NC – No Internal Connection
Positive logic: See Truth Table

μA9616

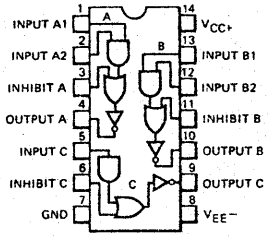
TRIPLE EIA RS-232-C LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA9616 is a Triple Line Driver which meets the electrical interface specifications of EIA RS-232-C and CCITT V.24. Each driver in the μA9616 converts TTL/DTL logic level to EIA/CCITT levels for transmission between data terminal equipment and data communication equipment. The μA9617 performs the complementary functions. The output slew rate is internally limited and can be lowered by an external capacitor; all output currents are short circuit limited. The outputs are protected against RS-232-C fault conditions. A logic HIGH level on the inhibit terminal interrupts signal transfer and forces the output to a $-V_{OUT}$ or MARK state. The μA9616 is constructed on a single silicon chip using the Fairchild Planar* process.

- INTERNAL SLEW RATE LIMITING
- NO EXTERNAL CAPACITORS REQUIRED
- THREE CHANNELS PER PACKAGE
- MEETS EIA RS-232-C AND CCITT V.24 SPECIFICATIONS
- LOGICAL TRUE INHIBIT FUNCTION
- SUPPLY INDEPENDENT OUTPUT SWING
- OUTPUT CURRENT LIMITING

CONNECTION DIAGRAM
(TOP VIEW)



TRUTH TABLE

INPUT 1	INPUT 2	INHIBIT	OUTPUT
All Sections:			
L	L	L	H
H	H	L	L
L	L	H	L
H	H	H	L
For Channels A & B add:			
L	H	L	H
H	L	L	H
L	H	H	L
H	L	H	L

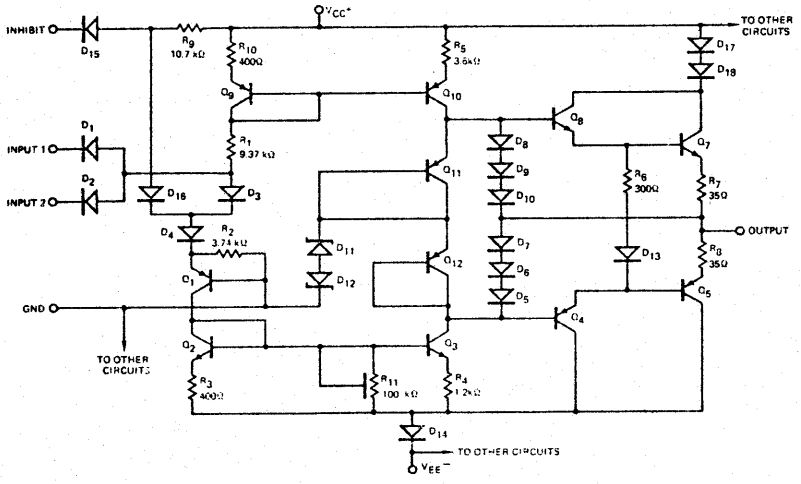
(For Channel C, omit INPUT 2 Column)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±15 V
Input or Inhibit Voltage	−1.5 to +6 V
Output Signal Voltage	±15 V
Maximum Power Dissipation (Note 1)	630 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature	0°C to +75°C
Lead Temperature (Soldering, 60 seconds)	300°C

Note 1: Perate 8.3mW/°C above 70°C

EQUIVALENT CIRCUIT (One of three channels)



*Planar is a patented Fairchild process.

μA9617

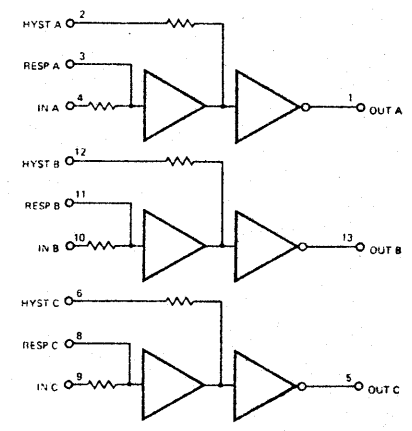
TRIPLE EIA RS-232-C LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA9617 is a Triple Line Receiver designed to meet the terminator electrical requirements of EIA RS-232-C AND CCITT V.24. It receives line signals produced by the μA9616, an EIA/CCITT driver, and converts them to TTL compatible logic levels. The inputs have a resistance between 3 kΩ and 7 kΩ and can withstand ±25 V. Each receiver can operate in either hysteresis or non-hysteresis (slicing) modes, and each receiver provides fail-safe operation as defined by Section 2.5 of RS-232-C. Noise immunity may be increased by connecting a capacitor between the response control pin and ground. The μA9617 is constructed on a single silicon chip using the Fairchild Planar* process.

- **MEETS ALL EIA RS-232-C AND CCITT V.24 SPECIFICATIONS**
- **FAIL-SAFE OPERATION**
- **HYSTERESIS OR NON-HYSTERESIS MODE**
- **INDIVIDUAL RESPONSE CONTROLS**
- **TTL COMPATIBLE OUTPUT**
- **SINGLE +5 V SUPPLY**

LOGIC DIAGRAM



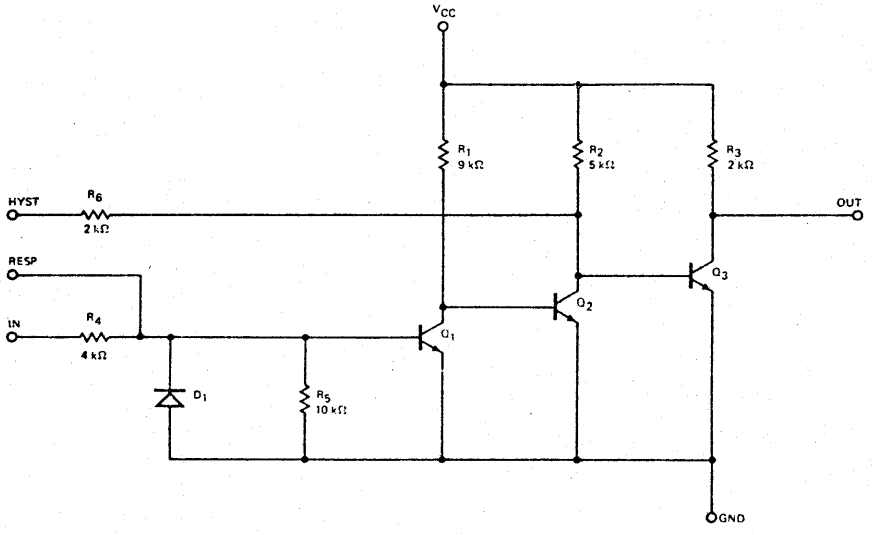
V_{CC} = Pin 14
GND = Pin 7

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7 V
Input Voltage	±25V
Output Current	25 mA
Maximum Power Dissipation (Note 1)	630mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +75°C
Lead Temperature (Soldering, 60 seconds)	300°C

Note 1. Derate 8.3 mW/°C above 70°C

EQUIVALENT CIRCUIT (One of three identical circuits)



*Planar is a patented Fairchild process.

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REVISIONS					
ZONE	LTR	EO NO.	DESCRIPTION	DATE	APPROVED
8D6A	A	1034	UPDATED REF DES C1-C4, U15-6	8-9-78	[illegible]

NOTES:

QTY	PART NUMBER	DESCRIPTION	MANUFACTURER	CODE IDENT	REF DES	ITEM

PARTS LIST

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.X ± .06
.XX ± .02
.XXX ± .010
ANGULAR ± .5 DEG

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

MATERIAL

NEXT ASSY | USED ON

APPLICATION

CONTRACT NO.

SIGNATURES	DATE
DR B McClarney	1-18-78
DES	
CHK E. McCain	8-9-78
ENGR Wallace Berry	5-31-78
APP	
APP	

TEXAS ELECTRONIC INSTRUMENTS, INC
HOUSTON, TEXAS

3P+3S I/O SCHEMATIC

SIZE	CODE IDENT NO.	DWG NO.	REV
D	33179	13224	A

SCALE | REL EO NO. | SHEET | OF

5-19

TEI INC.

5075 S. Loop East
Houston, Texas 77033

713-738-2300
TWX: 1-910-881-3639

SECTION VI
MCS-FDC PC BOARD
(FLOPPY DISK CONTROLLER)
TEI INC.

P/N 13686-6

SECTION VI

TEI, INC. MCS-FDC PC BOARD

FLOPPY DISK CONTROLLER

		PAGE
A.	THEORY	
	1. GENERAL DESCRIPTION	6-2
	2. FD1771 COMMANDS	6-3
	3. PORTS USED	6-4
	4. SYSTEM MEMORY	6-4
	5. IC CHIP LIST	6-4
	7. VOLTAGE REGULATOR LIST	6-5
B.	SOFTWARE	
	1. TYPE 1 COMMANDS	6-6
	2. TYPE 2 COMMANDS	6-6
	3. TYPE 3 COMMANDS	6-6
	4. COMMAND SUMMARY	6-7
	5. FLAGS: TYPE 1, 2, 3	6-7
	6. FLAGS: TYPE 4	6-8
	7. PORT 85 (HEX) DRIVE SELECT COMMAND	6-8
	8. INTERFACE CONNECTIONS	6-11
C.	HARDWARE	
	1. FDC 2 (S/N 201 and following)	
	a. Parts list	6-12
	b. Component layout drawing	6-13
	c. Schematic diagram	6-15
	2. FDC 1 (S/N 101 to 200)	
	a. Parts list	6-17
	b. Component layout drawing	6-18
	c. Schematic diagram	6-19

FLOPPY DISK CONTROLLER (MCS-FDC)

GENERAL:

S100 INTERFACE STANDARD AND MINI DRIVE CONTROL, SINGLE AND DOUBLE-SIDED. ALL CARDS ARE DESIGNED TO OPERATE WITH THE 8080A PROCESSOR. SPECIAL PROMS ALLOW OPERATION WITH 8080 OR Z80A 2 OR 4 MHZ. ALL DISK I/O SOFTWARE ROUTINES ARE PROVIDED. CONSULT SOFTWARE MANUAL FOR PARAMETER PASSING AND SUBROUTINE CALLS.

BASIC DESCRIPTION:

THE TEI DISK CONTROLLER UTILIZES THE WESTERN DIGITAL FD1771 LSI CONTROLLER CHIP. ALL INPUT/OUTPUT SIGNALS ARE FULLY BUFFERED FROM THE S100 BUS. THIS BOARD WILL SUPPORT 8 STANDARD DISK DRIVES AND 3 MINI DISK DRIVES. FORMAT COMES FACTORY SET FOR SOFT SECTORED, 128 BYTE SECTOR LENGTH (IBM 3740 FORMAT).

FEATURES:

DISK READ/WRITE TIMING INDEPENDENT OF SYSTEM CLOCK (ON CARD 4MHz CRYSTAL)

SOFTWARE CONTROLLED DRIVE SELECTION (STANDARD DRIVE (2MHz) OR MINI DRIVE (1MHz))

SUPPORTS SCHUGART 800, 850, 400, OR 450 DRIVES (SINGLE OR DOUBLE SIDED DISKETTES)

ON CARD PROMS (2 2708 TYPE E PROMS) FOR DISK-I/O CONTROL AND SYSTEM I/O.

OPTIMIZED TIMING FOR MINIMUM DISK ACCESS TIME.

AUTOMATIC CYCLIC REDUNDANCY CHECK (X↑16+X↑12+X↑5+1)

THE FD1771 WILL ACCEPT AND EXECUTE ELEVEN COMMANDS:

RESTORE	GO TO TRACK 00
SEEK	SEARCH FOR THE GIVEN TRACK AND SECTOR)
STEP	STEP ONE TRACK (SAME DIRECTION AS LAST STEP
STEP IN	STEP TOWARDS TRACK 76
STEP OUT	STEP TOWARDS TRACK 00
READ	READ THE GIVEN SECTOR (SINGLE OR MULTIPLE SECTORS)
WRITE	WRITE THE GIVEN SECTOR (SINGLE OR MULTIPLE SECTORS)
READ ADDRESS	READ THE PRESENT DISK ID FIELD
READ TRACK	READ THE GIVEN ENTIRE TRACK
WRITE TRACK	WRITE THE GIVEN ENTIRE TRACK
FORCE INTERRUPT	TERMINATE THE CURRENT COMMAND UNDER EXECTION AND INTERRUPT

OTHER PROGRAMMABLE FUNCTIONS:

- SECTOR LENGTH 16, 32, 48, 64, 128,,,,,,,,,,,,,4096 BYTES PER SECTOR
- NON-IBM FORMATS
- HEAD LOAD TIMING
- TRACK STEP TIMING
- SYNCHRONIZE TO ADDRESS MARK (OR NOT TO)
- AUTOMATIC TRACK SEEK WITH VERIFICATION OR NO VERIFICATION
- AUTOMATIC TRACK REGISTER UPDATE OR NO UPDATE

PORTS USED:

PORT	READ	WRITE
80 (HEX)	STATUS REGISTER	COMMAND REGISTER
81 (HEX)	TRACK REGISTER	TRACK REGISTER
82 (HEX)	SECTOR REGISTER	SECTOR REGISTER
83 (HEX)	DATA REGISTER	DATA REGISTER
84 (HEX)	HEAD LOAD STATUS	DRIVE SELECT REGISTER

SYSTEM MEMORY USED:

U25	PROM #1	F000=F3FF (HEX)	DISK I/O
U21	PROM #2	F400-F7FF (HEX)	SYSTEM I/O

I. C. CHIPS USED:

U1	7405	HEX INVERTER	LOGIC CONTROL (OPEN COLLECTOR)
U2	7432	QUAD 2-INPUT OR GATE	LOGIC CONTROL (PORT SELECT/READ-WRITE)
U3	74125	QUAD LINE DRIVER (TRI-STATABLE)	CLOCK LOGIC (MINI/STANDARD DRIVE)
U4	74LS08	QUAD 2-INPUT AND GATE	DATA SEPARATION CIRCUIT
U5	7404	HEX INVERTER	DATA SEPARATION AND CLOCK CIRCUIT
U6	74LS161	BINARY COUNTER	DATA SEPARATION CIRCUIT
U7	74LS175	QUAD D-FLIP-FLOP	DATA SEPARATION CIRCUIT
U8	74LS00	QUAD 2-INPUT NAND GATE	DATA SEPARATION CIRCUIT AND WRITE FAULT LOGIC
U9	NE555	TIMER CHIP	MINI-DRIVE MOTOR ON TIMING (APPROX. 4 SEC.)
U10	74121	ONE-SHOT MULTIVIBRATOR	HEAD LOAD TIMMING
U11	74LS04	HEX INVERTER	DISK READY, RAW DATA, READ/WRITE, & FORMAT CONTROL LOGIC
U12	74LS02	QUAD 2-INPUT NOR GATE	READ/WRITE-PROM & PORT SELECT LOGIC
U13	74LS00	QUAD 2-INPUT NAND GATE	READ/WRITE-PROM & DRIVE TYPE SELECT LOGIC
U14	7404	HEX INVERTER	ADDRESS DECODE & INTERRUPT CIRCUIT
U15	7407	HEX BUFFER	READ/WRITE - INTERRUPT - DISK INPUT LOGIC
U16	7406	HEX INVERTER (OPEN COLLECTOR)	DISK DRIVE LOGIC (OUTPUT)
U17	74LS74	DUAL D FLIP-FLOP	DATA SEPARATION CIRCUIT
U18	7438(FDC2)	QUAD 2- INPUT NAND BUFFER	
	7401(FDC1)	QUAD 2-INPUT NAND GATE	MINI-DISK DRIVE SELECT & HEAD LOAD STATUS LOGIC
U19	74164	8-BIT SERIAL TO PARALLEL	MINI-DISK READY LOGIC

I.C. CHIPS USED (CONT):

U20	DM8131	6-BIT BUS COMPARATOR	PORT DECODE LOGIC
U21	2708	EPROM	SYSTEM I/O SOFTWARE
	8131 (FDC2)	6-BIT UNIFIED BALL COMPARATOR	
U22	7430 (FDC1)	8-INPUT NAND GATE	PROM ADDRESS DECODE LOGIC
U23	FD1771	LSI FLOPPY DISK CONTROLLER	
U24	8212	8-BIT LATCH	DISK DRIVE SELECT LATCH/BIT CONTROL
U25	2708	EPROM	DISK CONTROL SOFTWARE
U26	74367	BUS DRIVER	ADDRESS BUFFERS
U27	74367	BUS DRIVER	ADDRESS BUFFERS
U28	8T26A	BUS DRIVER	DATA BUFFERS
U29	8T26A	BUS DRIVER	DATA BUFFERS
U30	8212	8-BIT LATCH	INTERRUPT AND DISABLE INTERRUPT AND RESTART BIT GENERATOR
*U31	7406	HEX INVERTER (OPEN COLLECTOR)	DISK DRIVE LOGIC(OUTPUT)
*U32	7406	HEX INVERTER (OPEN COLLECTOR)	DISK DRIVE LOGIC(OUTPUT)
	*FDC2 ONLY		
		VOLTAGE REGULATORS:	
Q1	7805	5 VOLT REGULATOR	TTL LOGIC SUPPLY (Vcc)
CR1	IN751A	ZENER DIODE -5.1 VOLTS	PROM & 1771 POWER
CR2	IN759A	ZENER DIODE +12 VOLTS	PROM & 1771 POWER

SOFTWARE:

TYPE 1 COMMANDS: RESTORE, SEEK, STEP, STEP-IN, AND STEP OUT

STATUS FOR TYPE 1 COMMANDS:

S7	DISK NOT READY	WHEN SET INDICATES THE DISK DRIVE IS NOT READY.
S6	PROTECTED	WHEN SET INDICATES WRITE PROTECT IS ACTIVATED.
S5	HEAD LOAD	WHEN SET IT INDICATES THE HEAD IS LOADED AND ENGAGED.
S4	SEEK ERROR	WHEN SET INDICATES THAT THE DESIRED TRACK WAS NOT VERIFIED.
S3	CRC ERROR	WHEN SET THERE WAS ONE OR MORE CRC ERRORS.
S2	TRACK ØØ	WHEN SET INDICATES THAT THE READ/WRITE HEAD IS AT TRACK ØØ.
S1	INDEX	WHEN SET INDICATES INDEX MARK DETECTED FROM DRIVE.
SØ	BUSY	WHEN SET COMMAND IS IN PROGRESS.

TYPE 2 COMMANDS: READ, WRITE

TYPE 3 COMMANDS: READ ADDRESS, READ TRACK, WRITE TRACK

STATUS FOR TYPE 2 AND 3 COMMANDS:

S7	NOT READY	WHEN SET INDICATES THE DRIVE IS NOT READY.
S6	RECORD TYPE	ON READ RECORD, INDICATES THE MSB OF RECORD-TYPE CODE FROM DATA FIELD ADDRESS MARK.
	WRITE FAULT	WHEN SET INDICATES A WRITE FAULT.
S5	RECORD TYPE	ON READ RECORD, INDICATES THE LSB OF RECORD-TYPE CODE FROM DATA FIELD ADDRESS MARK.
	WRITE FAULT	ON WRITE TRACK, INDICATES A WRITE FAULT.
S4	RECORD NOT FOUND	WHEN SET INDICATES THAT THE DESIRED TRACK AND SECTOR WAS NOT FOUND.
S3	CRC ERROR	WHEN SET INDICATES ONE OR MORE ERRORS ENCOUNTERED.
S2	LOST DATA	WHEN SET INDICATES THE COMPUTER DID NOT RESPOND TO DRQ IN ONE BYTE TIME.
S1	DATA REQUEST	WHEN SET INDICATES THE DATA REGISTER IS FULL ON A OPERATION, OR THE DATA REGISTER WAS EMPTY ON A WRITE OPERATION.
SØ	BUSY	WHEN SET INDICATES THAT A COMMAND IS UNDER EXECUTION

NOTE: FORCE INTERRUPT IS A TYPE 4 COMMAND.

FDC COMMAND SUMMARY

TYPE	COMMAND	7	6	5	4	3	2	1	0	BITS
1	RESTORE	0	0	0	0	h	V	r1	r2	
1	SEEK	0	0	0	1	h	V	r1	r2	
1	STEP	0	0	1	u	h	V	r1	r2	
1	STEP IN	0	1	0	u	h	V	r1	r2	
1	STEP OUT	0	1	1	u	h	V	r1	r2	
2	READ	1	0	0	m	b	E	0	0	
2	WRITE	1	0	1	m	b	e	a1	a0	
3	READ ADDRESS	1	1	0	0	0	1	0	0	
3	READ TRACK	1	1	1	1	0	1	0	s	
3	WRITE TRACK	1	1	1	1	0	1	0	0	
4	FORCE INTERRUPT	1	1	0	1	I3	I2	I1	I0	

TYPE 1 FLAGS:

h= HEAD LOAD FLAG — H= 1 LOAD HEAD AT BEGINNING; h= 0 DO NOT LOAD HEAD AT BEGINNING

V =VERIFY FLAG — V= 1 VERIFY ON LAST TRACK; V= 0 NO VERIFY

r1, r0 = STEPPING MOTOR RATE

0	0	= 6msec. STEP PULSE
0	1	6msec.
1	0	10msec.
1	1	20msec.

NOTE: THE ABOVE TIMES ARE FOR A 2MHz CLOCK (DOUBLE THESE TIMES FOR THE MINI-DISK)

TYPE 2 FLAGS:

m = MULTIPLE RECORD — m = 0 SINGLE RECORD; m = 1 MULTIPLE RECORD

BLOCK LENGTH — b = 0 NON-IBM FORMAT (16 to 4096 bytes); b = 1 IBM FORMAT (128 to 1024 bytes)

a1	a0	DATA ADDRESS MARK
0	0	FB (DATA MARK)
0	1	FA (USER DEFINED)
1	0	F9 (USER DEFINED)
1	1	F8 (DELETED DATA MARK)

TYPE 3 FLAGS:

s = SYNCHRONIZE FLAG — s = 0 SYNCHRONIZE TO AM; s = 1 DO NOT SYNCHRONIZE TO AM

TYPE 4 FLAGS:

I1 = INTERRUPT CONDITION FLAGS

- IØ = 1 NOT READY TO READY TRANSITION
- I1 = 1 READY TO NOT READY TRANSITION
- I2 = 1 INDEX PULSE
- I3 = 1 IMMEDIATE INTERRUPT

E = ENABLE HEAD LOAD AND 10 msec DELAY

- E = 0 HEAD IS ASSUMED ENGAGED AND THERE IS NO DELAY
- E = 1 ENABLE HLD, HLT AND 10 msec DELAY

PORT 85 (HEX) DRIVE SELECT COMMANDS
SA800/SA850

BIT	FUNCTION
0	DRIVE ENABLE (SELECT CIRCUIT)
1	DRIVE SELECT LOGIC BIT (MULTIPLEX SIGNAL)
2	DRIVE SELECT LOGIC BIT
3	DRIVE SELECT LOGIC BIT

DRIVE		BIT 0	1	2	3
	A	0	1	1	1
	B	0	0	1	1
	C	0	1	0	1
	D	0	0	0	1
	E	0	1	1	0
	F	0	0	1	0
	G	0	1	0	0
	H	0	0	0	0
SA400/450	1 A	1	1	0	0
	2 B	1	0	1	0
	3 C	1	0	0	1

4	SIDE SELECT (SA850 & SA450) H = Side 0 L = Side 1
5	DOOR LOCK (SA450 ONLY)
6	SOFTWARE WRITE PROTECT 1 = PROTECT
7	DRIVE SELECT TYPE H = MINI DRIVE L = STANDARD DRIVE

REV A: Revised SA400/450 Bit Table

CPU BIT PATTERNS FOR DRIVE SELECT

	DRIVE	BIT	0	1	2	3
SA-800	A		1	0	0	0
	B		1	1	0	0
	C		1	0	1	0
	D		1	1	1	0
	E		1	0	0	1
	F		1	1	0	1
	G		1	0	1	1
	H					

FDC-2
T-DOS 1.41

* SA-400/SA-450
SAME AS PAGE 6-8

SA-800
SA-850

AFTER SEPTEMBER 6, 1978
FDC-2
T-DOS 1.42

	A		0	1	0	0
	B		0	0	1	0
	C		0	0	0	1
	D		1	0	0	0
SA-400	A		X	1	0	0
SA-450	B		X	0	1	0
	C		X	0	0	1

Bits 4, 5 and 7 same as page 8
Bit 6 high = write protect
soft ware controled
Cut Jumper HP
Jumper SP

MCS-FDC

INTERFACE CONNECTIONS:

J1 50 PIN RIBBON CABLE FOR SA800 OR SA850 DISK DRIVES

PIN NO.	FUNCTION
1	GND - GROUND (ALL ODD NUMBER PINS GROUND)
14	SIDE SELECT (SA850 DRIVE)
18	HEAD LOAD
20	INDEX PULSE
22	DISK READY
26	ENABLE DRIVE SELECT
28	DRIVE SELECT
30	DRIVE SELECT
32	DRIVE SELECT
34	DIRECTION
36	STEP
38	WRITE DATA
40	WRITE GATE
44	WRITE PROTECT
46	RAW DATA FROM DISK
48	SEPARATED DATA (NA)
50	SEPARATED CLOCK (NA)

J2 34 PIN CONNECTOR SA400 OR SA450 DISK DRIVE (MINI-DRIVE)

1	GND - GROUND (ALL ODD NUMBER PINS GROUND)
4	DOOR LOCK (SA450 ONLY)
8	INDEX PULSE
10	DRIVE SELECT DISK A
12	DRIVE SELECT DISK B
14	DRIVE SELECT DISK C
16	MOTOR ON (NOTE: HEAD LOADS WITH MOTOR ON)
18	DIRECTION
20	STEP PULSE
22	WRITE DATA
24	WRITE GATE
26	TRACK 00
28	WRITE PROTECT
30	RAW DATA FROM DISK

TEI INC.

PARTS LIST

MCS-FDC 2 BOARDS

REF DES	DESCRIPTION	TEI P/N
C1 thru C7	Cap, 10mf @ 20V	1580-001
C8 thru 25	Cap, .1mf	1562-002
C26	Cap, 30 pf	1551-002
CR1	Diode IN751A	4840-004
CR2	Diode IN759	4840-001
CR3,CR4	Diode IN916	4825-009
J1	50 Pos. Edge Conn.	2125-020
J2	34 Pos. Edge Conn.	2125-012
Q1	Regulator, 7805	3120-003
R1	RES 150 Ω 1 W 10%	4727-258
R2	RES 33 Ω 1/2 W 10%	4725-195
R3, R4, R10	RES 910 Ω 1/4 W 2%	4741-333
R5, R13 thru R15, R30, R33 thru R36		
R39	RES 4.7K 1/4 W 2%	4741-402
R6, R7, R8, R9, R32	RES 10K 1/4 W 2%	4741-433
R11,R12	RES 560 Ω 1/4 W 2%	4741-313
R16, R17 R18thruR20 R23,27,28	RES 270 Ω 1/4 W 2%	4741-283
R21,22	RES 220 Ω 1/4 W 2%	4741-274
R29,24,26	RES 330 Ω 1/4 W 2%	4741-291
R31	RES 390K 1/4 W 2%	4741-586
U1	IC Chip 7405	3161-001
U2	IC Chip 7432	3161-006
U3	IC Chip 74125	3161-008
U4	IC Chip 74LS08	3164-020
U5	IC Chip 7404	3161-016
U6	IC Chip 74LS161	3164-012
U7	IC Chip 74LS157	3164-016
U8,U13	IC Chip 74LS00	3164-002
U9	IC Chip NE555	3100-001
U10	IC Chip 74121	3161-030
U11,U14	IC Chip 74LS04	3164-007
U12	IC Chip 74LS02	3164-004
U15	IC Chip 7407	3161-002
U16	IC Chip 7406	3161-028
U17	IC Chip 74LS74	3164-003
U18	IC Chip 7438	3161-042
U19	IC Chip 74164	3161-041
U20	IC Chip 8131	3160-004
U21*U25*	IC Chip 2708	3163-005
U22	IC Chip 8131	3160-004
U23	IC Chip 17718	3160-017
U24,U30	IC Chip 8212	3162-001
U26,U27	IC Chip 74367	3161-003

REF DES	DESCRIPTION	TEI P/N
U28, U29	IC Chip 8T26	3160-018
Y1	Crystal 4.000 MHZ	2300-004
U31,U32	IC Chip 7406	3161-028

*OPTIONAL

REVISIONS					
ZONE	LTR	EO NO.	DESCRIPTION	DATE	APPROVED

J1 50 PIN
J2 34 PIN
* OPEN COLLECTOR

U1 — 7405	U8,U13 — 74LS00	U17 — 74LS74	U26,U27 — 74367
U2 — 7432	U9 — NE555	U18, — 74 38	U28,U29 — 8T26
U3 — 74125	U10 — 74121	U19 — 74164	
U4 — 74LS08	U11, — 74LS04	U20 — 8131	U21,U25 — 2708(OPTIONAL)
U5 — 7404	U12 — 74LS02	U22 — 8131	U14 — 74LS04
U6 — 74LS161	U15 — 7407	U23 — 1771B	U32 — 7406
U7 — 74LS175	U16,U31 — 7406	U24,U30 — 8212	

NOTES:

QTY	PART NUMBER	DESCRIPTION	MANUFACTURER	CODE IDENT	REF DES	ITEM

PARTS LIST

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.X ± .06
.XX ± .02
.XXX ± .010
ANGULAR ± .5 DEG

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

MATERIAL

CONTRACT NO.

SIGNATURES	DATE
DR DM Clarney	12-27-77
DES LAST REV	3-28-78
CHK	
ENGR Wallace Barnes	3-20-78
APP	
APP	

NEXT ASSY	USED ON
	MCS-FDC

APPLICATION

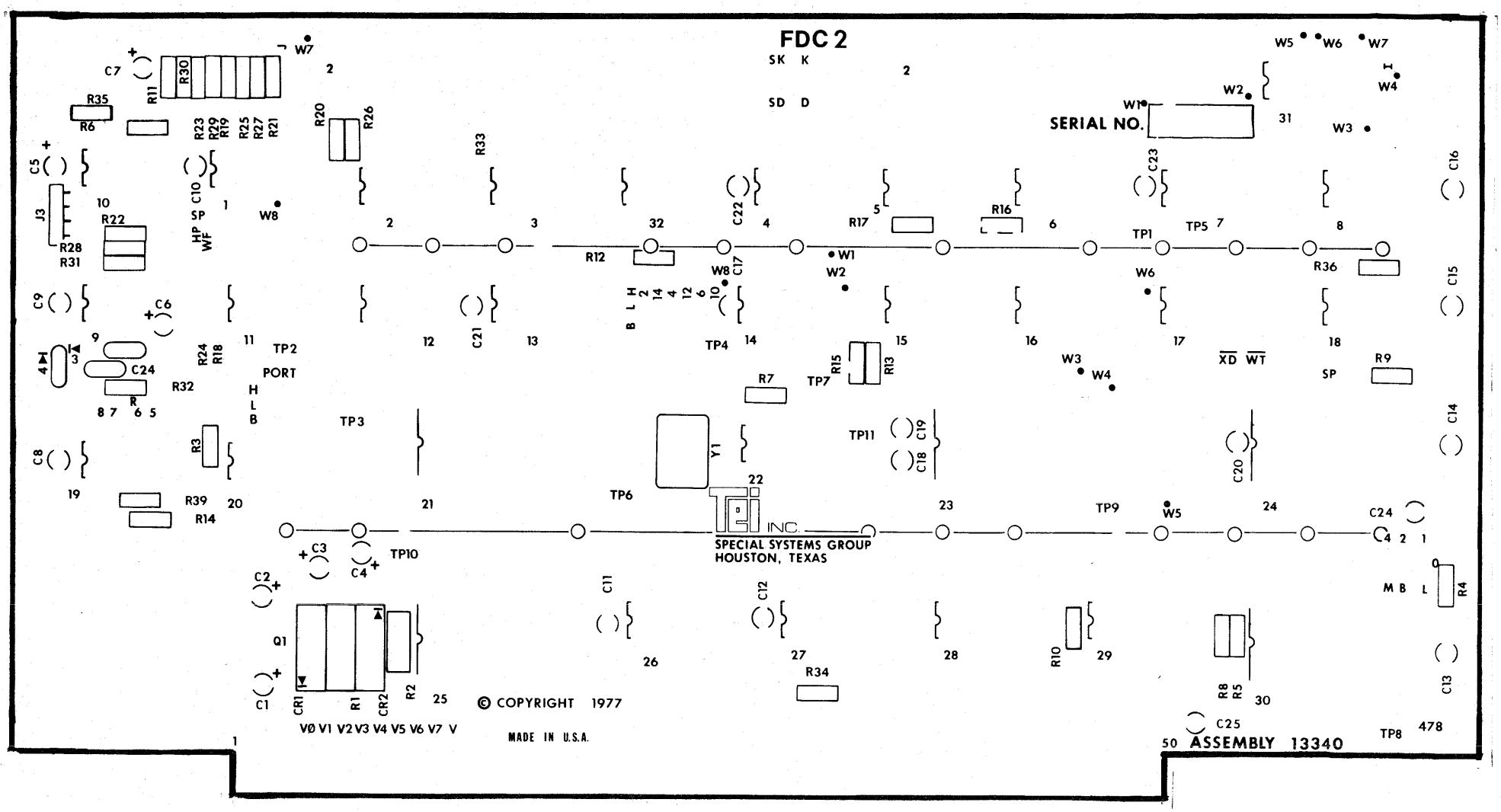
TEXAS ELECTRONIC INSTRUMENTS, INC
HOUSTON, TEXAS

MCS-FDC 2
FLOPPY DISK CONTROLLER BOARD

SIZE	CODE IDENT NO.	DWG NO.	REV
D	33179	13539	C
SCALE	REL EO NO.	SHEET 1 OF 1	

DWG NO. 13539 REV

6-13



MCS-FDC COMPONENT LAYOUT FOR BOARDS S/N 201 and following

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TEI INC.

PARTS LIST

MCS-FDC Board

REF DES	DESCRIPTION	TEI P/N
C1 thru C7	Cap, 10 Mf @ 20V	1580-001
C8 thru C16, C17 thru C23	Cap, .1Mf	1562-002
C24	Cap, 30 Pf	1551-002
CR1	Diode IN751A	4840-004
CR2	Diode IN759	4840-011
CR3	Diode IN916	4825-009
J1	50 Pos. Edge Conn.	2125-020
J2	34 Pos. Edge Conn.	2125-012
Q1	Regulator, 7805	3120-003
R1	RES 150 Ω 1 W 10%	4727-258
R2	RES 33 Ω 1/2 W 10%	4725-195
R3, R4, R10 thru R15, R30, R33 thru R36	RES 910 Ω 1/4 W 2%	4741-333
R5, R13	RES 4.7K 1/4 W 2%	4741-402
R6, R7, R8, R9, R32	RES 10K 1/4 W 2%	4741-433
R11,R12	RES 560 Ω 1/4 W 2%	4741-313
R16, R17	RES 270 Ω 1/4 W 2%	4741-283
R18 thru R23	RES 220 Ω 1/4 W 2%	4741-274
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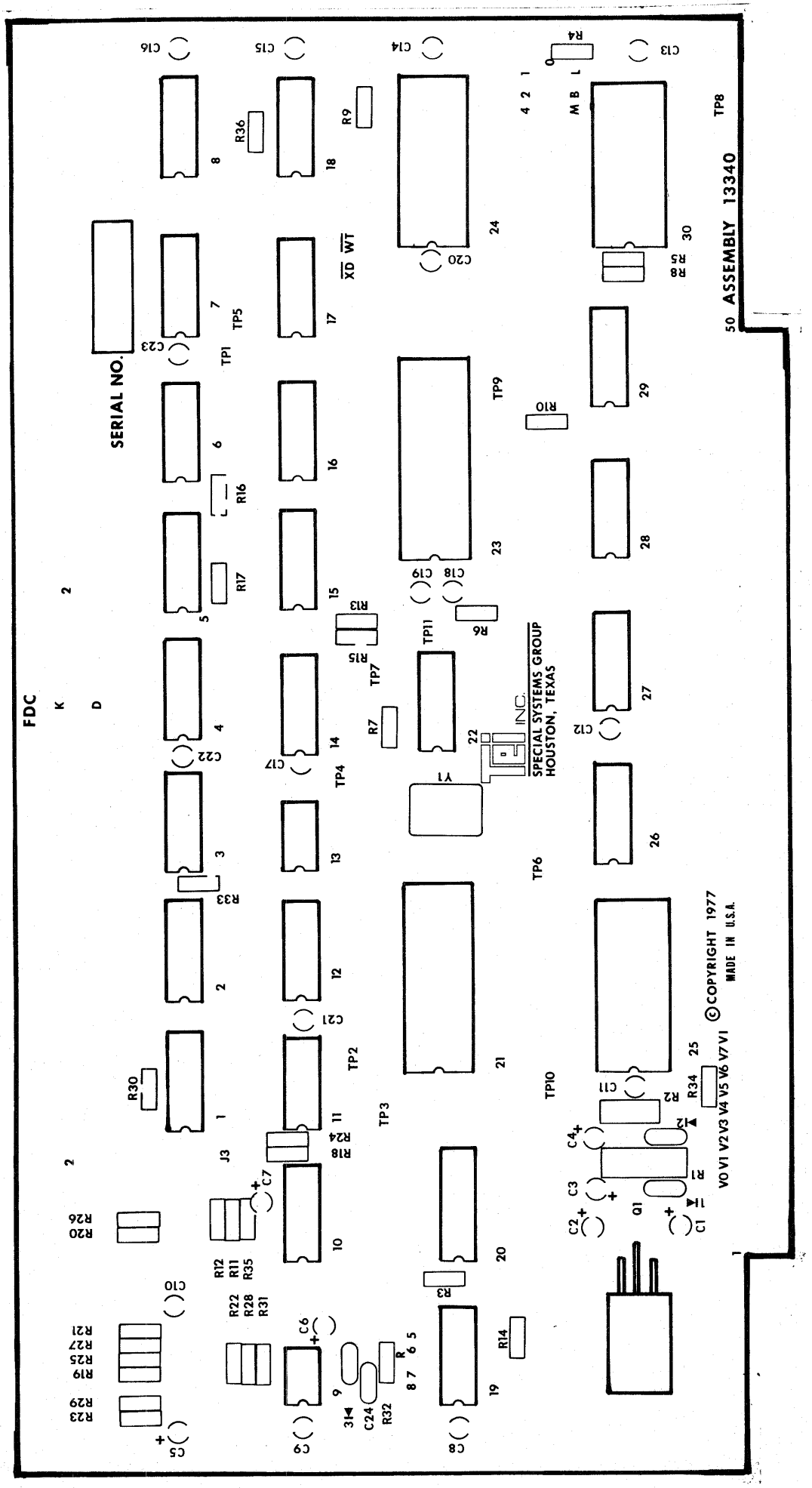
R31	RES 390K 1/4 W 2%	4741-586
U1	IC Chip 7405	3161-001
U2	IC Chip 7432	3161-006
U3	IC Chip 74125	3161-008
U4	IC Chip 74LS08	3164-020
U5	IC Chip 7404	3161-016
U6	IC Chip 74LS161	3164-012
U7	IC Chip 74LS175	3164-016
U8, U13	IC Chip 74LS00	3164-002
U9	IC Chip NE555	3100-001
U10	IC Chip 74121	3161-030
U11, U14	IC Chip 74LS04	3164-007
U12	IC Chip 74LS02	3164-004
U15	IC Chip 7407	3161-002
U16	IC Chip 7406	3161-028
U17	IC Chip 74LS74	3164-003
U18	IC Chip 7401	3161-021
U19	IC Chip 74164	3161-041
U20	IC Chip 8131	3160-004
U21* U25*	IC Chip 2708	3163-005
U22	IC Chip 74LS30	3164-005
U23	IC Chip 1771B	3160-017
U24, U30	IC Chip 8212	3162-001
U26, U27	IC Chip 74367	3161-003
U28, U29	IC Chip 8T26	3160-018
Y1	Crystal 4.000 MHZ	2300-004

*OPTIONAL



MCS-FDC COMPONENT LAYOUT FOR BOARDS S/N 101 thru 200

TEI INC.

5075 S. Loop East
Houston, Texas 77033

713-738-2300
TWX: 1-910-881-3639

SECTION VII
MCS-RAM 16K PC BOARD
TEI INC.

SECTION VII

MCS - RAM 16K

		PAGE
1.	THEORY OF OPERATION	7-3
2.	PARTS LIST (4200 SERIES)	7-6
3.	PARTS LIST (6104 SERIES)	7-6
4.	COMPONENT LAYOUT (4200 SERIES)	7-7
5.	COMPONENT LAYOUT (6104 SERIES)	7-8
6.	SCHEMATIC DIAGRAM (4200 SERIES)	7-9
7.	SCHEMATIC DIAGRAM (6104 SERIES)	7-11

TEI, INC. 16K RAM BOARD -4200 STATIC RANDOM ACCESS MEMORY-
DESIGNED FOR THE S100 BUS
LOW POWER - NO WAIT STATES
8080 OR Z80

EMM/SEMI 4200 RAM CHIPS ARE ORGANIZED IN AN ARRAY OF 64 ROWS BY 64 COLUMNS (4096 X 1 BIT). WHEN CHIP SELECT IS HIGH ALL PINS ARE IN AN INOPERATIVE HIGH IMPEDANCE STATE, AND POWER IS SUPPLIED ONLY TO THE MEMORY ELEMENTS. THE MEMORY CELLS (BECAUSE THEY ARE CROSS COUPLED HIGH IMPEDANCE STATIC CELLS) WILL RETAIN DATA DOWN TO Vdd = 4 VOLTS DC. THE NORMAL VOLTAGE LEVEL FOR Vdd IS 12 VOLTS DC. THERE IS AN APPROXIMATE 10 TO 1 REDUCTION IN POWER CONSUMPTION DURING THE ACTIVE TO STANDBY MODE OF OPERATION. DATA WILL BE VALID EXCEPT FOR THE MOST SEVERE BROWN-OUT CONDITIONS.

THE 4200 CHIP REQUIRES 3 SUPPLY VOLTAGES +5, -5, AND +12 VDC. DUE TO BOARD ORGANIZATION, ONLY ONE 4K BLOCK OF RAM AT ANY GIVEN TIME IS ACTIVE IN SYSTEM MEMORY RESULTING IN EXTREMELY LOW POWER CONSUMPTION. THIS GREATLY EASES SYSTEM GENERATED HEAT AND POWER LOSS. TYPICALLY RAM IS THE LARGEST CURRENT DEMAND IN ANY GIVEN SYSTEM.

FEATURES:

S-100 BUS 4MHz OPERATION
VERY LOW POWER 620MA +5 320MA +12 96MA -5
SOLDER MASK SILK SCREEN PLATED THROUGH HOLES

EACH 4K BLOCK ADDRESSABLE TO ANY 4K BOUNDARY
EACH 16K CARD ADDRESSABLE TO ANY ONE OF 16 PAGES

A TOTAL OF 256K MAY BE ADDRESSED TO THE SAME LOCATION
64 4K BLOCKS MAY BE ADDRESSED TO THE SAME LOCATION

FULLY BUFFERED
BOARD WILL ALSO SUPPORT NEC 410 MEMORY CHIPS.
PHANTOM PIN 67 OF S-100 BUS IMPLEMENTED.

FUNCTIONAL DESCRIPTION:

ADDRESS SELECT

EACH 4K BLOCK IS REPRESENTED BY P0, P1, P2, AND P3.

MEMORY ADDRESSES ARE IN INCREMENTS OF 4K BLOCKS. BY JUMPERING P0 TO BLOCK 0 SETS THE FIRST 4K BLOCK TO MEMORY LOCATION 0000 HEX. P1 TO 4 SETS THE NEXT 4K BLOCK TO MEMORY LOCATION 4000 HEX. P2 TO 8 SETS THE NEXT 4K BLOCK TO MEMORY LOCATION 8000 HEX. P3 TO 12 SETS THE NEXT 4K BLOCK TO MEMORY LOCATION 6000 HEX - ENDING AT 7FFF HEX. THIS BOARD NOW OCCUPIES THE FIRST 16K OF RAM 0000 - 3FFF HEX.

THE ABOVE EXAMPLE ASSUMES THAT PAGE SELECT IS IN THE DEFAULT MODE P0, P1, P2, AND P3 MAY BE JUMPERED TO ANY ONE OF 16 POSITIONS (0,4,8,12,16,20, 24,28,32,36,40,44,48,52,56,60) WHICH COVERS THE NORMAL RANGE OF 0 TO 64K.

ADDRESS SELECT	HEX ADDRESS		
0	0000	0FFF	
4	1000	1FFF	
8	2000	2FFF	
12	3000	3FFF	
16	4000	4FFF	
20	5000	5FFF	
24	6000	6FFF	
28	7000	7FFF	
32	8000	8FFF	
36	9000	9FFF	
40	A000	AFFF	
44	B000	BFFF	
48	C000	CFFF	
52	D000	DFFF	
56	E000	EFFF	
60	F000	FFFF	TOP OF MEMORY 64K

THE DECODE CHIP FOR THE ABOVE ADDRESS IS A 74154. THIS IS A 1 OF 16 DECODE CHIP WHICH LOOKS AT THE HIGH ORDER 4 BITS AND DETERMINES WHICH 4K BLOCK IS BEING ADDRESSED BY THE MICROPROCESSOR. IC 40 A 7474 FLIP-FLOP, SUPPLYS THE NECESSARY TIMING FOR THE 4200 CHIP BY DECODING PSYNC, PHASE 1 CLOCK, AND IS RESET BY SMEMR. IC 49 AND IC 35 SERVE TO CREATE THE ON-CARD READ WRITE SIGNAL, AND TO EXTEND THE ADDRESS DECODE ENABLE SIGNAL CREATED BY THE 7474 FLIP-FLOP. THE IN916 DIODE IS USED TO INSURE THAT DURING A MEMORY READ THE DATA OUT (MEMORY BOARD) BUFFER IS IN CONTROL OF THE CHIP ENABLE FOR ADDRESS DECODE UNTIL THE ADDRESS BUS GOES NOT TRUE. ONCE A READ CYCLE IS STARTED IT IS KEPT ACTIVE UNTIL THE ADDRESS BUS BIT PATTERN CHANGES STATE.

IC 46 AND 39 (SMEMR AND POBIN) IS USED TO CREATE THE ON CARD MEMORY READ SIGNAL. IF MEMORY READ IS TRUE (ACTIVE LOW) AND ADDRESS DECODE IS TRUE AND PAGE SELECT IS TRUE THEN A MEMORY READ IS ACTIVATED.

WHEN MEMORY WRITE (BUS SIGNAL M WRITE-PIN 68) IS TRUE, AND ADDRESS DECODE IS TRUE, AND PAGE SELECT IS TRUE THEN A MEMORY WRITE IS ACTIVATED. DURING THIS MODE THE 7474 FLIP-FLOP IS NOT THE PRIMARY SIGNAL SOURCE FOR THE FUNCTION.

PAGE SELECT

IC 44 (74154) IS USED FOR PAGE SELECT. THIS IS A ONE OF SIXTEEN DECODE CHIP. DATA TO BE DECODED IS STORED IN A SINGLE 74175 (LATCH) BY OUT-PUTTING TO PORT 7F (HEX). ONLY THE UPPER 4 BITS ARE USED TO CONTROL THE PAGE SELECT. PAGE ZERO IS THE DEFAULT MODE AS SHIPPED FROM THE FACTORY. IC 41 (74LS30) DECODES THE LOWER 8 BITS OF THE ADDRESS BUS AND WHEN BUS SIGNAL "SOUT" AND "PWR" ARE TRUE DATA IS LATCHED INTO THE 74175.

EXAMPLE BIT PATTERNS FOR PAGE SELECT

PAGE SELECTED	BIT 7	BIT 6	BIT 5	BIT 4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	0	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

FOR THE ABOVE PAGE SELECTION BIT CODES THE PAGE SELECT JUMPERS P0, P1, P2, AND P3 ARE IN THE DEFAULT MODE. JUMPER P0 TO P1 TO P2 TO P3 TO NP ---- NP THEN JUMPERS TO ONE OF THE 16 DECODE BITS OF THE 74154 LABELED 0 THRU 15.

NOTE: THE JUMPER LABELED 16K ALSO MUST BE JUMPERED. THIS IS THE MODE AS SHIPPED FROM THE FACTORY. NP IS JUMPERED TO DECODE BIT 0. SEE SCHEMATIC DRAWING 13564.

BANK/PAGE SELECT

IC 42 (74175) IS USED TO LATCH IN THE LOWER 4 BITS OF THE DATA BUS IN THE SAME MANNER THAT IC 43 ABOVE FUNCTIONS USING PORT 7F (HEX). THE PURPOSE OF THE 4 BITS IS TO CONTROL WHICH OF THE 4 4K BLOCKS OF RAM IS TO BE ACTIVE WHEN THE JUMPERS LABELED PAGE SELECT ARE JUMPERED TO THE 74175 (IC 42). THIS OPTION ALLOWS THE USER TO JUMPER ALL 4 4K BLOCKS OF MEMORY TO THE SAME 4K ADDRESS IN SYSTEM MEMORY AND THEN USE THE ONE OF SIXTEEN DECODER (BANK SELECT) AND PAGE SELECT THRU THE LOW ORDER 4 BITS TO SELECT ANY ONE OF 64 4K BLOCKS OF MEMORY ADDRESSED TO THE SAME LOCATION IN MEMORY. SINCE 64 COMBINATIONS IS QUITE LENGTHLY, NO EXAMPLE IS GIVEN.

IC 38 IS USED TO DECODE ADDRESS TRUE AND PAGE/BANK SELECT TRUE.

IC 37 DETECTS ONE OF 4 CHIP SELECT SIGNALS AND WHEN ANDED WITH MEMORY READ GATES DATA ONTO THE DATA BUS FOR A READ MODE.

IC 35 CONVERTS THE TTL SIGNAL TO THE 0 TO 12 VOLT SIGNAL NEEDED FOR THE 4200 RAM CHIP SELECT. CHIP SELECT IS ACTIVE LOW.

IC 47 AND 48 ARE ADDRESS BUS BUFFERS TO ISOLATE THE BOARD FROM THE SYSTEM BUS.

IC 49 AND 50 ARE USED TO BUFFER THE INCOMING DATA FROM THE SYSTEM BUS.

IC 36 AND 51 ARE USED TO BUFFER THE DATA OUT TO THE SYSTEM BUS (DRIVER).

TEI INC.

PARTS LIST

MCS-16K RAM

4200 SERIES

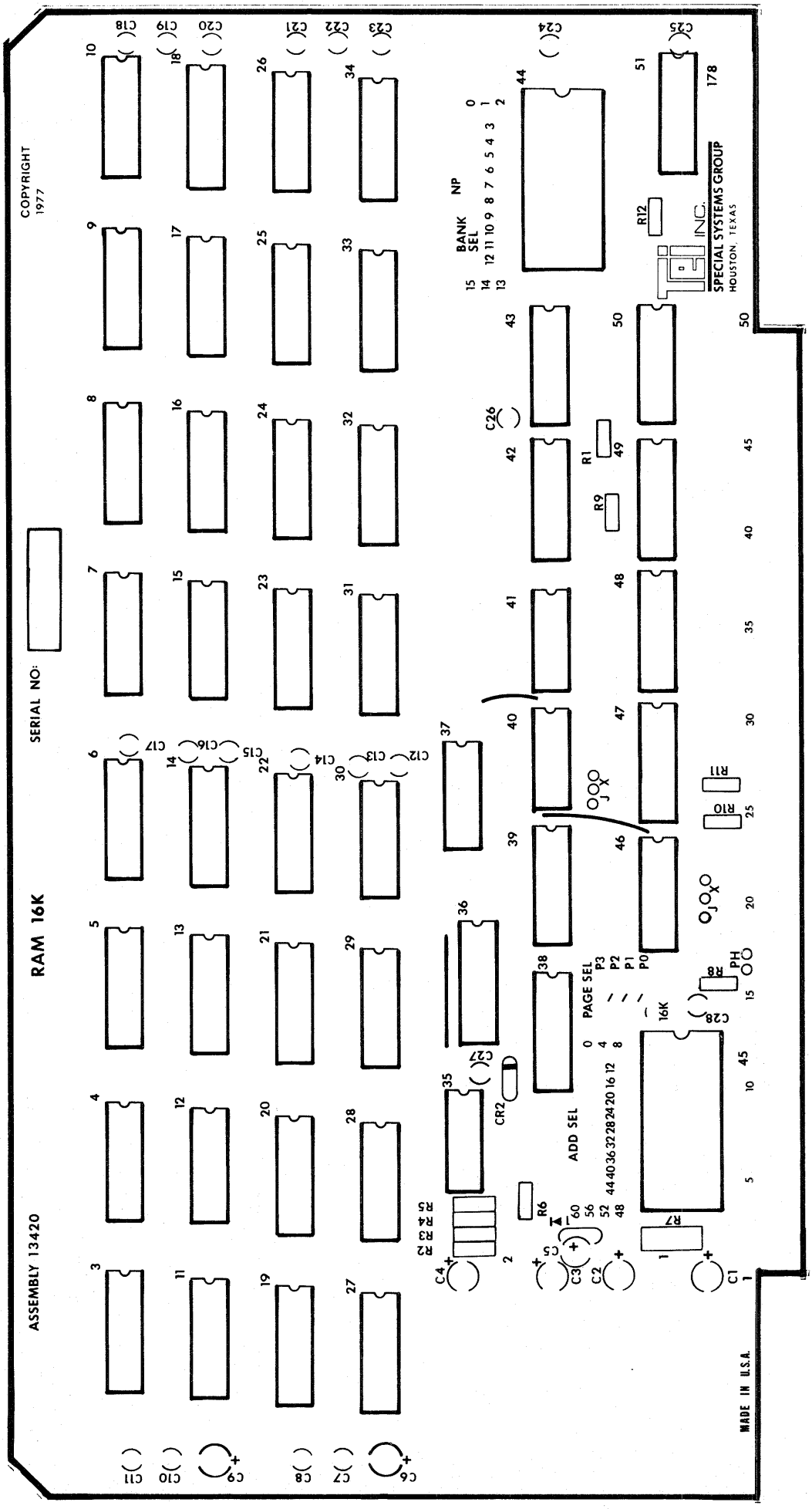
REF DES	DESCRIPTION	TEI P/N
C1 Thru C6		
C9, C25	Cap. 10MF, 20 VDC	1580-001
C7,8, C10 Thru 24		
C26,27,28	Cap, .1MF	1562-002
CR1	Diode 1N 751A	4840-004
CR2	Diode 1n 916	4825-009
R1	RES 150 Ω 1/4 W 2%	4741-258
R2 Thru R5		
R9,R12	RES 390 Ω 1/4 W 2%	4741-298
R6	RES 910 Ω 1/4 W 2%	4741-333
R7	RES 330 Ω 1/2 W 10%	4725-291
R8	RES 4.7K 1/4 W 2%	4741-402
R10,R11	RES 130 Ω 1/4 W 2%	4741-252
U1	Regulator 7805	3120-003
U2	Regulator 7812	3120-007
U3 Thru		
U34	IC Chip RAM 4200	3163-003
U35	IC Chip 7406	3161-028
U36, U46,		
U51	IC Chip 74LS368	3164-029
U37	IC Chip 74LS21	3164-026
U38	IC Chip 74LS32	3164-027
U39	IC Chip 7432	3161-006
U40	IC Chip 7474	3161-020
U41	IC Chip 74LS30	3164-005
U42, U43	IC Chip 74175	3161-027
U44, U45	IC Chip 74L154*	3166-002
U47 Thru		
U50	IC Chip LS367	3164-028
	Heat Sink	4890-002
	PCB FAB	13421

*U44, U45 Substitute: 74LS154 3164-008

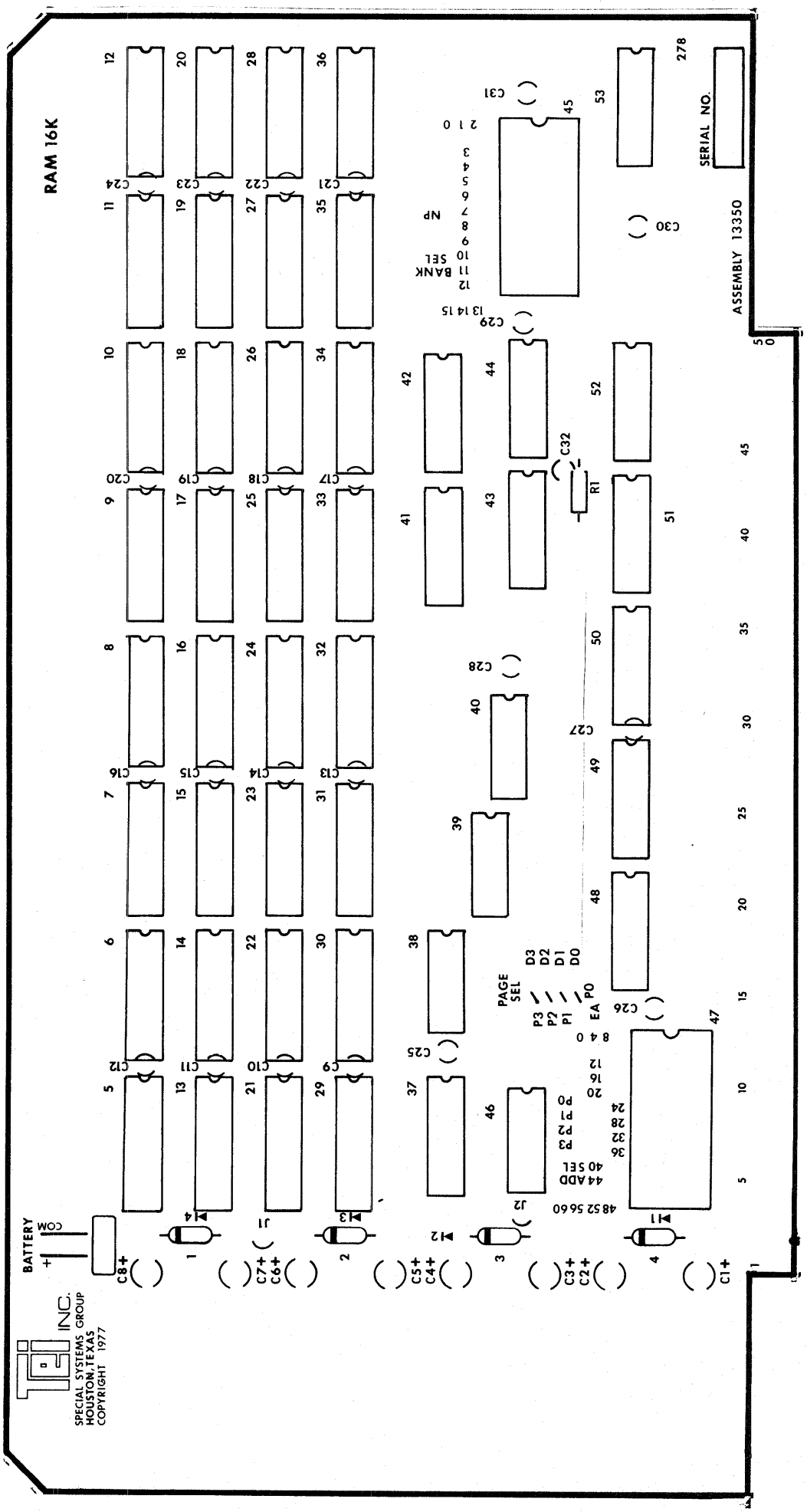
6104 SERIES

REF DES	DESCRIPTION	TEI P/N
C1 Thru C8	Cap 10MF, 20 VDC	1580-001
C9 Thru C32	Cap, .1MF	1562-002
R1	RES 150 Ω 1/4 W 2%	4741-258
U1 Thru U4	Regulator 7805	3120-003
U5 Thru U36	IC Chip RAM 6104-4	3163-009
U37	IC Chip 74LS367	3164-028
U38	IC Chip 74LS21	3164-026
U39, U44	IC Chip 74LS32	3164-027
U40	IC Chip 74LS30	3164-005
U41, U42	IC Chip 74LS175	3164-016
U43, U45	IC Chip 74LS154	3164-008
U46	IC Chip 74LS368	3164-029
U47 Thru		
U51	IC Chip 74LS367	3164-028
	Heat Sink, Regulator	4890-003
	PCB FAB.	13351

MCS- RAM 16K (4200) COMPONENT LAYOUT



MCS-RAM 16K (6104) COMPONENT LAYOUT



TEI INC.
SPECIAL SYSTEMS GROUP
HOUSTON, TEXAS
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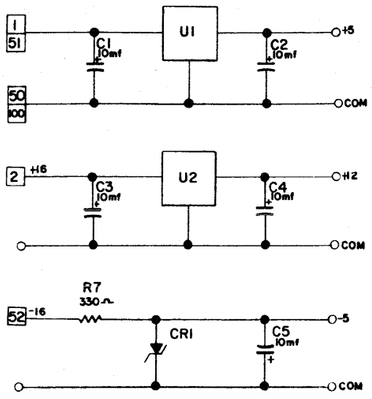
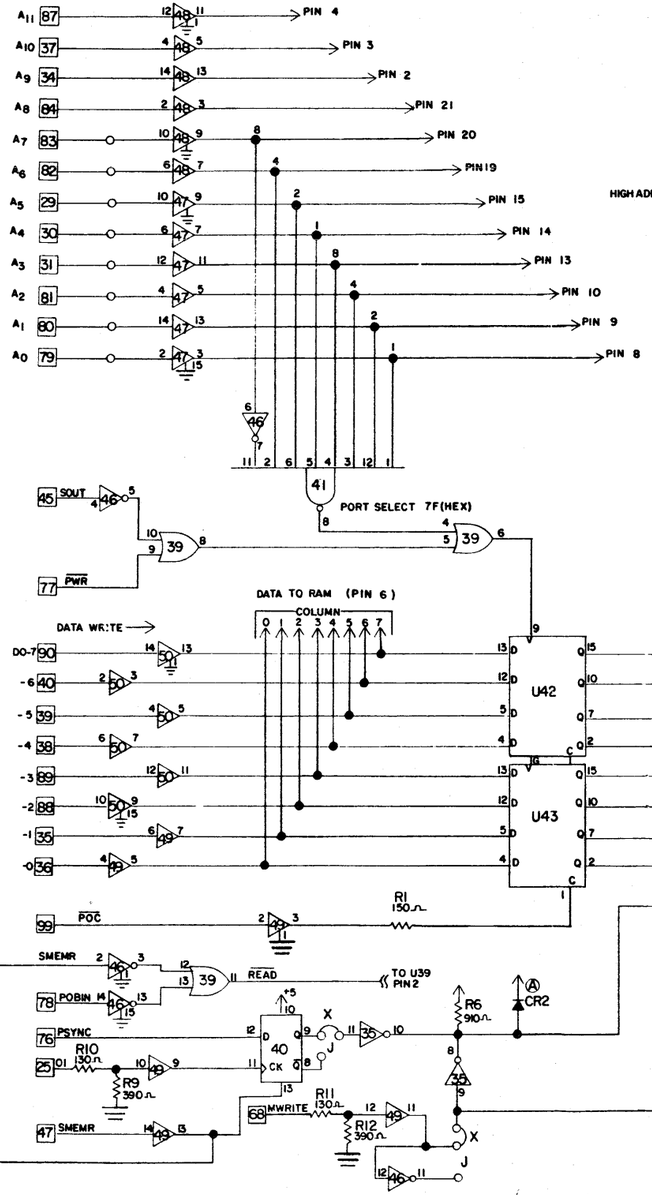
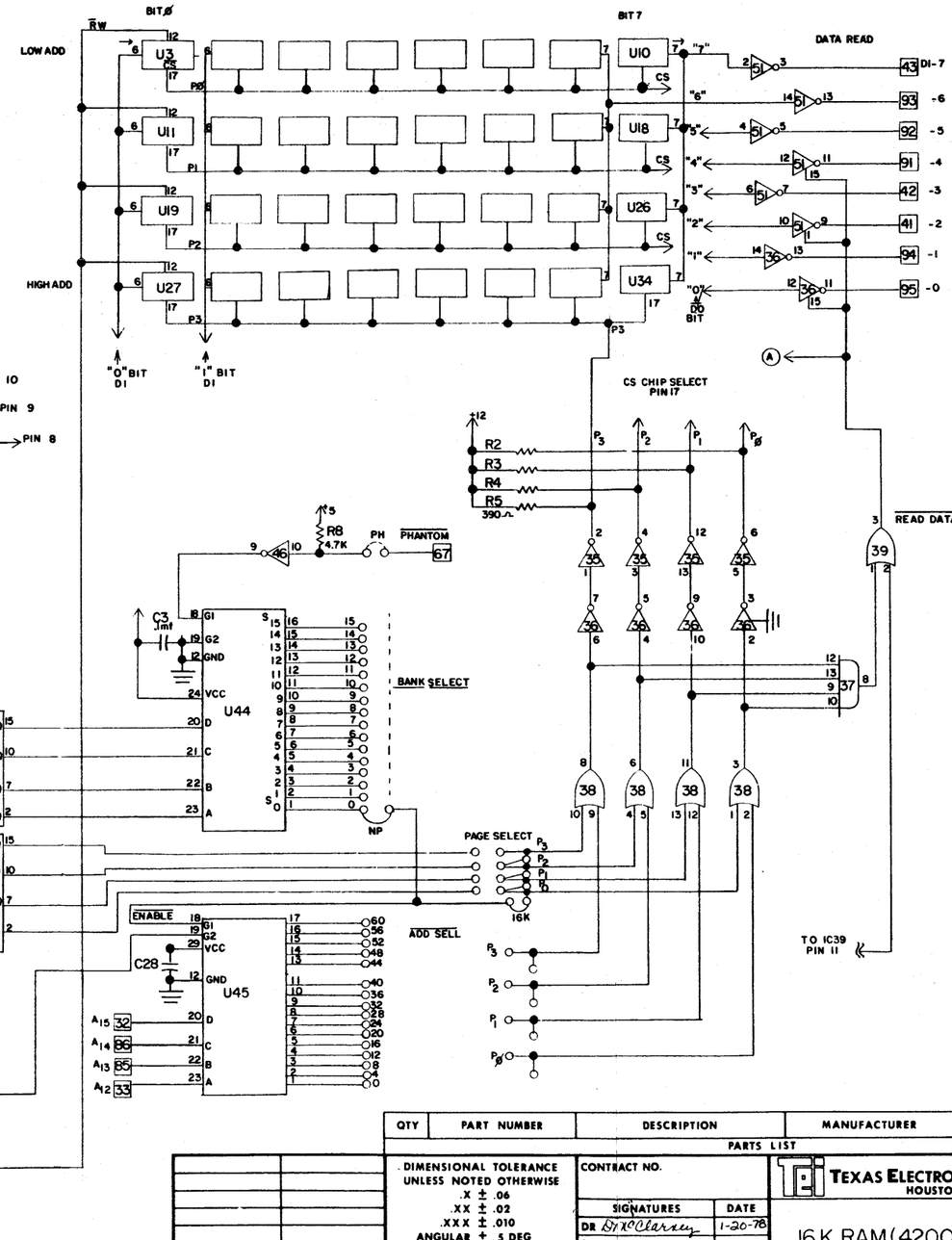
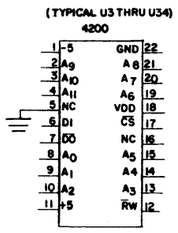
REVISIONS					
ZONE	LTR	EO NO.	DESCRIPTION	DATE	APPROVED
	A	1034	CORRECTED PIN NUMBERING	8-9-78	EME

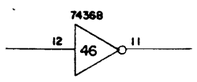


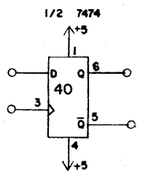




(TYPICAL U3 THRU U34)
4200







QTY	PART NUMBER	DESCRIPTION	MANUFACTURER	CODE IDENT	REF DES	ITEM

PARTS LIST

NEXT ASSY | USED ON

APPLICATION

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.X ± .06
.XX ± .02
.XXX ± .010
ANGULAR ± .5 DEG

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

MATERIAL

CONTRACT NO.

SIGNATURES	DATE
DR Dix McClarney	1-20-78
DES	
CHK D. Haviza	4-4-78
ENGR William Berry	4-4-78
APP	
APP	

TEXAS ELECTRONIC INSTRUMENTS, INC
HOUSTON, TEXAS

16K RAM(4200) SCHEMATIC

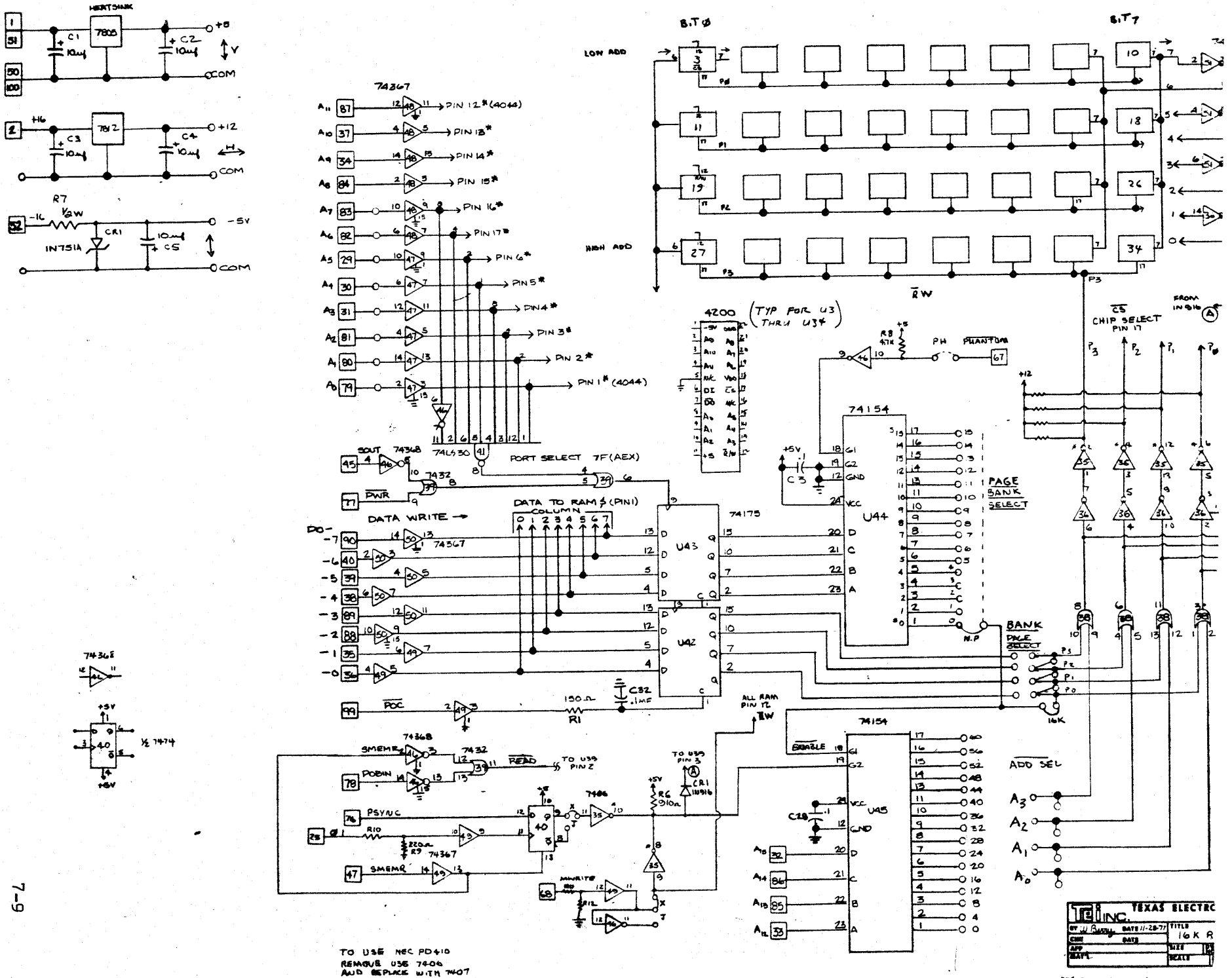
SIZE	CODE IDENT NO.	DWG NO.	REV
D	33179	13564	A

SCALE | REL EO NO. | SHEET 1 OF 1

DWG NO. 13564 REV A

NOTES:

7-9


HEATSINK
7805
C1
10uf
C2
10uf
+5
COM
7812
C3
10uf
C4
10uf
+12
COM
R7
1/2W
CR1
IN751A
C5
10uf
-5V
COM
74367
PIN 12* (4044)
PIN 13*
PIN 14*
PIN 15*
PIN 16*
PIN 17*
PIN 6*
PIN 5*
PIN 4*
PIN 3*
PIN 2*
PIN 1* (4044)
74LS30
74348
7432
PWR
PORT SELECT 7F(AEX)
DATA WRITE
DATA TO RAM (PIN1)
COLUMN
0 1 2 3 4 5 6 7
74175
U43
U42
C32
.1MF
150Ω
R1
POC
74368
SMEMR
POBIN
PSYNC
R10
220Ω
R9
SMEMR
MWRITE
READ
TO U39 PIN 2
TO U39 PIN 3
7406
R6
510Ω
CR1
1N916
ALL RAM PIN 12
RW
74154
ENABLE
U45
C28
.1
A10
A14
A15
A12
ADD SEL
A3
A2
A1
A0
B.TØ
B.T7
LOW ADD
HIGH ADD
4200
(TYP FOR U3 THRU U3*)
R8
4.7K
PH
PHANTOM
67
74154
U44
C3
.1
PAGE BANK SELECT
N.P
BANK PAGE SELECT
16K
CS
CHIP SELECT PIN 17
FROM IN 916
74365
½ 7474
TO USE NEC PD410
REMOVE U36 7406
AND REPLACE WITH 7407
CUT X
JUMPER J
TEI INC.
TEXAS ELECTRO
BY W Austin
DATE 11-28-77
TITLE
16K R
CHK
DATE
APP
SIZE
DRAFT
SCALE

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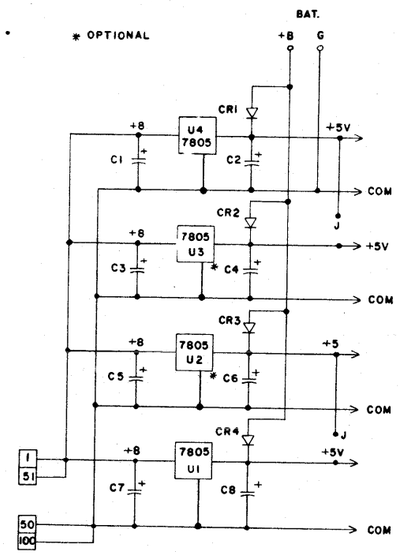
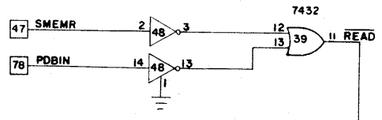
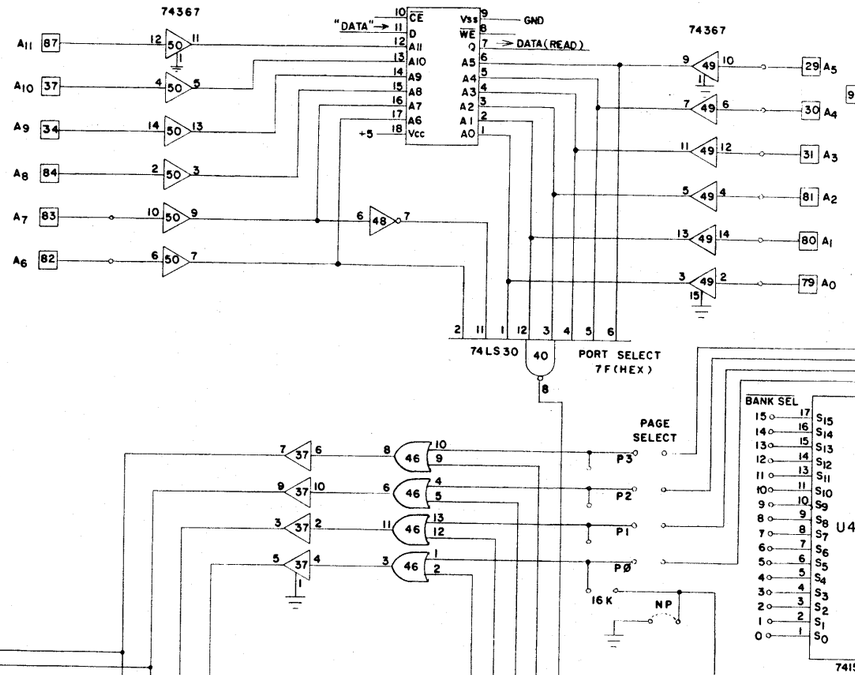
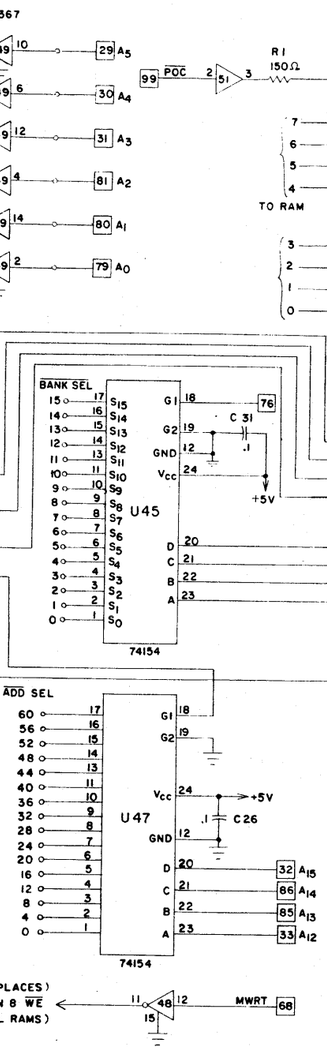
REVISIONS					
ZONE	LTR	EO NO.	DESCRIPTION	DATE	APPROVED
	A	1034	UPDATED LABELING	8-9-78	

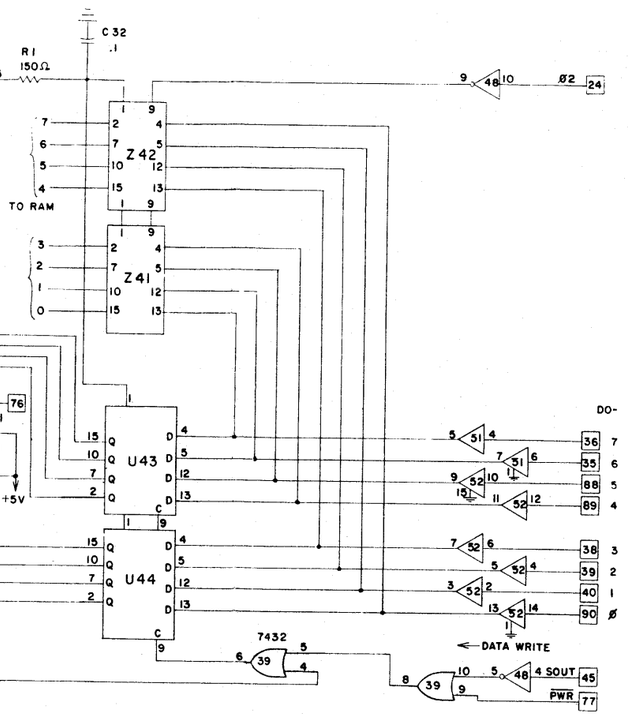






IC U5-36
4044 X 32





IC	P/N
1	7805
2*	7805
3*	7805
4	7805
5-36	TI 4044(4K RAM)
37	74367
38	74 LS 21
39	74 LS 32
40	74 LS 30
41,42	74 LS 175
43,44	74 LS 175
45	74 LS 154
46	74 LS 32
47	74154
48	74368
49	74367
50	74367
51	74367
52	74367
53	74367
54	74367

*OPTIONAL

NOTES:

QTY	PART NUMBER	DESCRIPTION	MANUFACTURER	CODE IDENT	REF DES	ITEM

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.X ± .06
.XX ± .02
.XXX ± .010
ANGULAR ± .5 DEG

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

MATERIAL

CONTRACT NO.

SIGNATURES	DATE
DR TMB	3-29-78
DES	
CHK D. Marrujo	4-9-78
ENGR Mike Berry	4-4-78
APP	
APP	

TEXAS ELECTRONIC INSTRUMENTS, INC
HOUSTON, TEXAS

SCHEMATIC

16K RAM (4044)

SIZE	CODE IDENT NO.	DWG NO.	REV
D	33179	13386	A

SCALE | REL EO NO. | SHEET 1 OF 1

7-11

TEI INC.

5075 S. Loop East
Houston, Texas 77033

713-738-2300
TWX: 1-910-881-3639

SECTION VIII
MCS-VCB PC BOARD
(VIDEO CONTROLLER BOARD)
TEI INC.

SECTION VIII

TEI, INC. MCS-VCB

TABLE OF CONTENTS

		PAGE
1.	THEORY OF OPERATION	
	(A) CLOCKS AND TIMING	8-2
	(B) 5027 CRT CONTROLLER	8-2
	(C) CURSOR GENERATOR	8-3
	(D) SCREEN MEMORY	8-3
	(E) CHARACTER GENERATION	8-3
	(F) OPTIONS	8-4
	(G) FIGURE 1	8-5
	(H) FIGURE 2	8-6
	(I) FIGURE 3	8-7
	(J) FIGURE 4	8-8
	(K) FIGURE 5	8-9
2.	COMPONENT LAYOUT	8-10
3.	PARTS LISTS	8-11
4.	IC LIST	8-12
5.	SCHEMATIC	8-13

VIDEO CONTROLLER BOARD (VCB) THEORY OF OPERATION:

(A) Clocks and Timing:

Two inverter gates and a 22.225 MHZ crystal make up the system clock. The system clock frequency determines the width of the individual dots in the characters. The MCS-VCB uses a 5x7 dot matrix for the character format. There are 2 dot spaces between characters making an effective character width of 7 dots. Because of this a new character must be loaded every 7 dot clock cycles. A 74163(Z39) is used as a divide by 7 counter. Every nine dot clocks the 74163 provides a pulse to the 74121 (Z14). It is used to widen the pulse to 200 ns in the low states. The 5027 then increments the character counter by one and loads a new character into the 6061 character generator. Another 74121(Z29) is used to create a load signal to the shift register. It is triggered by the output of the 74163 and provides a load clock which is approximatly 2 dot clocks long. This enables the data transfer from the character generator (Z2) to the shift register.

(B) 5027 CRT CONTROLLER:

The 5027 is a user programable 40 pin LSI device containging the logic functions required to generate all the timing signals for the presentation and formating of interlaced and non interlaced video data. All SYNC signals (vertical, horizontal, and composite), characters per line, data rows per frame and raster scans per data row and per frame are user programable. Programing is accomplished through 6, (8 bit) control registers (Ports 90-95 HEX). See Figures 1, 2 & 3 for more details. The cursor position is determined by outputing cursor line number to port 9D (HEX) and cursor charactor position to port 9C (HEX). For example, if you wanted the cursor in the 3rd line and 40th character position, then output a Ø3 to port 9D (HEX) and a 28H (HEX) or 40 (DEC) to port 9C (HEX). The other control registers which are used in the MCS-VCB are:

9B (HEX): Any time this port is read or written to, the 5027 will scroll the data on the screen, i.e. Before scroll command top line = 0, bottom line = 23 after scroll command top line = 1, bottom line = 0.

9A (HEX): Any time this port is read or written to the 5027 will halt all timing.

9E (HEX): By accessing this port the CRT will start the timing if in a reset mode (if port 9A (HEX) has been previously accessed.

(C) Cursor Generation:

The cursor may be as a block cursor, blinking or not, or an underline cursor, also blinking or non blinking. As described previously, the corsor line position is loaded into port 9D (HEX) and cursor character position is loaded into port 9C (HEX). The 5027 controller generates a logic "high" on pin 16 each time it accesses the memory location that corresponds to the line and character position in the cursor registers during screen refresh. This in turn is translated into the cursor on the CRT.

(D) Screen Memory:

There are 2k bytes of memory allocated for the CRT screen. This memory is shared by the CPU and the 5027 CRT controler. This is accomplished through the use of 3 74157 multiplexer's. It is necessary that the CPU have control of the memory any time the screen needs to be up-dated. When the CPU accesses the screen memory, a wait state is generated in order for the character generation circuitry to finish what it is doing, and load a 2ØH (HEX) into the character generator. All of this is transparent to the CPU and the screen memory "looks" like any other RAM for both read and write. The screen memory may be addressed for any 2k block in memory and defaults to F8ØØ through FFFF. When the 5027 is programed for an 80 x 24 format it displays the RAM locations as 20 blocks of 64 bytes each. Block 1 is byte 1 to byte 64 (Figure D-1). Block 2 is byte 65 to byte 128. Block 20 is byte 1856 to byte 1920.

1	2	3	4	5
6	7	8	9	10
11	12	13	14	15
16	17	18	19	20

Screen Memory Map
in 64 BYTE sections

Figure D-1

(E) CHARACTER GENERATION:

The character generation is accomplished through the use of the 6061 character generator (Z10) and the 74166 shift register (Z11), Data from the screen memory is latched into the character generator by the load clock. A 5 bit word is loaded on the character generator outputs which is a function of the screen memory data and the row counter outputs of the 5027 (pins 8, 7, and 5). The character generator outputs are loaded in to the shift register on the next load clock. They are then shifted out serially on the next 5 dot clock cycles to form one line of one character. See Figures 4 & 5 for the character set of the character generator.

(F) Options:

(1) Underline cursor-defaults with no jumper.

(2) Block cursor-cut trace connected to left side of J9 and jumper J9.

(3) Blinking cursor-defaults with no jumper.

(4) Non-blinking cursor-cut trace which jumpers J3.

(5) Reverse video-
On composite video-jumper J10.
On seperated SYNC-Do Not jumper J10.

(6) Character-by-character reverse video.
On seperated SYNC-jumper J11, cut trace on J12.
Characters will be reverse on the 8th bit high.
On composite video the character will be reverse when the 8th bit is low.

(7) Composite video or seperated SYNC-see parts list.

(8) Screen memory location. The screen memory can be set to any 2k block of memory by jumpering the proper address line jumpers near the bottom left of the card. Jumper for the address line to be low.

Example: For screen memory at DØØØH.

A15 - No jumper
A14 - No jumper
A13 - Jumper
A12 - No jumper
A11 - Jumper

	A15	A14	A13	A12	A11
Binary					

FIGURE 1

CRT 5027 Control Registers Programming Chart

Horizontal Line Count: Total Characters/Line = N+1, N=0 to 225 (DBØ=LSB)

Characters/Data Row:

DB2	DB1	DBØ		
0	0	0	= 20	Active Characters/Data Row
0	0	1	= 32	
0	1	0	= 40	
0	1	1	= 64	
1	0	0	= 72	
1	0	1	= 80	
1	1	0	= 96	
1	1	1	= 132	

Horizontal Sync Delay: =N, from 1 to 7 character times (DBØ=LSB) (N=0 Disallowed)

Horizontal Sync Width: =N, from 1 to 15 character times (DB3=LSB) (N=0 Disallowed)

Skew Bits

DB6	DB7	Sync/Blank Delay (Character Times)	Cursor Delay
0	0	0	0
0	1	1	0
1	0	2	1
1	1	2	2

Scans/Frame

8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. (DBØ=LSB)

1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields.
Range = 513 to 1023 scans/frame, odd counts only.

2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011).
Range = 256 to 766 scans/frame, even counts only.

In either mode, vertical sync width is fixed at three horizontal scans (=3H).

Vertical Data Start: N= number of raster lines delay after leading edge of vertical sync of vertical start position. (DBØ=LSB)

Data Rows/Frame: Number of data rows = N+1, N=0 to 63 (DBØ=LSB)

Last Data Row: N= Address of last displayed data row, N=0 to 63, ie; for 24 data rows, program N=23. (DBØ=LSB)

Scans/Data Row: =N+1, N=0 to 15 (DB3=LSB)

TABLE 1

BIT ASSIGNMENT CHART

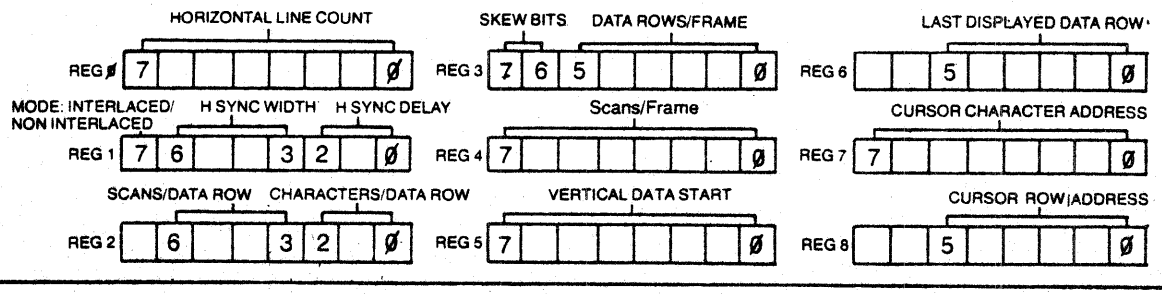


FIGURE 2

Register Selects/Command Codes

A3	A2	A1	AØ	Select/Command	Description
0	0	0	0	Load Control Register Ø	See Table 1
0	0	0	1	Load Control Register 1	
0	0	1	0	Load Control Register 2	
0	0	1	1	Load Control Register 3	
0	1	0	0	Load Control Register 4	
0	1	0	1	Load Control Register 5	
0	1	1	0	Load Control Register 6	
0	1	1	1	Processor Self Load	Command from processor instructing CRT 5027 to enter Self Load Mode
1	0	0	0	Read Cursor Character Address	
1	0	0	1	Read Cursor Line Address	
1	0	1	0	Reset	Resets timing chain to top left of page. Reset is latched on chip by $\overline{DS}$ and counters are held until released by start command.
1	0	1	1	Up Scroll	Increments address of first displayed data row on page. ie; prior to receipt of scroll command—top line = 0, bottom line = 23. After receipt of Scroll Command—top line = 1, bottom line = 0.
1	1	0	0	Load Cursor Character Address	
1	1	0	1	Load Cursor Line Address	
1	1	1	0	Start Timing Chain	Receipt of this command after a Reset or Processor Self Load command will release the timing chain approximately one scan line later. In applications requiring synchronous operation of more than one CRT 5027 the dot counter carry should be held low during the $\overline{DS}$ for this command.
1	1	1	1	Non-Processor Self Load	Device will begin self load via PROM when $\overline{DS}$ goes low. The 1111 command should be maintained on AØ-3 long enough to guarantee self load. (Scan counter should cycle through at least once). Self load is automatically terminated and timing chain initiated when the all "1's" condition is removed, independent of $\overline{DS}$. For synchronous operation of more than one CRT 5027, the Dot Counter Carry should be held low when this command is removed.

NOTE: During Self Load, the scan counter states corresponding to the nine load command addresses will load the appropriate register. Therefore if reseting of the cursor X and Y position registers is required via self load the PROM words for address 11ØØ and 11Ø1 should be programmed as all zeros.

FIGURE 3

Operation

The design philosophy employed was to allow the device to interface effectively with either a microprocessor based or hardwire logic system. The device is programmed by the user in one of two ways; via the processor data bus as part of the system initialization routine, or during power up via a PROM tied on the data bus and addressed directly by the Row Select outputs of the chip. (See figure 4). Seven 8 bit words are required to fully program the chip. Bit assignments for these words are shown in Table 1. The information contained in these seven words consists of the following:

Horizontal Formatting:	
Characters/Data Row	A 3 bit code providing 8 mask programmable character lengths from 20 to 132. The standard device will be masked for the following character lengths; 20, 32, 40, 64, 72, 80, 96, and 132.
Horizontal Sync Delay	3 bits assigned providing up to 8 character times for generation of "front porch".
Horizontal Sync Width	4 bits assigned providing up to 16 character times for generation of horizontal sync width.
Horizontal Line Count	8 bits assigned providing up to 256 character times for total horizontal formatting.
Skew Bits	A 2 bit code providing from a 0 to 2 character skew between the horizontal address counter and the horizontal blank and sync signals to allow for retiming of video data prior to generation of composite video signal. The Cursor Video signal is also skewed as a function of this code.
Vertical Formatting:	
Interlaced/Non-interlaced	This bit provides for data presentation with odd/even field formatting for interlaced systems. It modifies the vertical timing counters as described below.
Scans/Frame	8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. (DBØ=LSB) 1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields. Range = 513 to 1023 scans/frame, odd counts only. 2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011). Range = 256 to 766 scans/frame, even counts only. In either mode, vertical sync width is fixed at three horizontal scans (= 3H).
Vertical Data Start	8 bits assigned providing scan line resolution in vertical data positioning with respect to vertical sync. The Data Row Counter is reset at vertical sync and will not begin counting until the scan line selected by these eight bits.
Data Rows/Frame	6 bits assigned providing up to 64 data rows per frame.
Last Data Row	6 bits to allow up or down scrolling via a preload defining the count of the last displayed data row, ie: if DATA ROWS/FRAME is programmed for 24 data rows (see programming chart) and LAST DATA ROW is programmed for 15, the data row address sequence will appear from the top of page down as: 16 . . . . 23, 0 . . . . 15.
Scans/Data Row	4 bits assigned providing up to 16 scan lines per data row.

Additional Features

Device Initialization:

Under microprocessor control—The device can be reset under system or program control by presenting a Ø1Ø1 address on AØ-3. The device will remain reset at the top of the even field page until a start command is executed by presenting a Ø111 address on AØ-3.

Via "Self Loading"—In a non-processor environment, the self loading sequence is effected by presenting and holding the 1111 address on AØ-3, and is initiated by the receipt of the strobe pulse ($\overline{DS}$). The 1111 address should be maintained long enough to insure that all seven registers have been loaded (in most applications under one millisecond). The timing sequence will begin one line scan after the 1111 address is removed. In processor based systems, self loading is initiated by presenting the 111Ø address to the device. Self loading is terminated by presenting the start command to the device which also initiates the timing chain.

Scrolling—In addition to the Register 6 storage of the last displayed data row a "scroll" command (address 11Ø1) presented to the device will increment the first displayed data row count to facilitate up scrolling in certain applications.

A "FILLED IN" DOT REPRESENTS A LOW MEMORY OUTPUT

ASCII INPUT ADDRESS	$B_7B_6B_5$ $A_9A_8A_7$ 000 $O_5O_4O_3O_2O_1$	$A_9A_8A_7$ 001	$A_9A_8A_7$ 010	$A_9A_8A_7$ 011	$A_9A_8A_7$ 100	$A_9A_8A_7$ 101	$A_9A_8A_7$ 110	$A_9A_8A_7$ 111
$B_4B_3B_2B_1$ $A_6A_5A_4A_3$ 0000	(NUL)*	(DLE)*						
$A_6A_5A_4A_3$ 0001	(SOH)*	(DC1)*						
$A_6A_5A_4A_3$ 0010		(DC2)*						
$A_6A_5A_4A_3$ 0011	(ETX)*	(DC3)*						
$A_6A_5A_4A_3$ 0100	(EOT)*	(DC4)*						
$A_6A_5A_4A_3$ 0101	(ENQ)*	(NAK)*						
$A_6A_5A_4A_3$ 0110	(ACK)*	(SYN)*						
$A_6A_5A_4A_3$ 0111	(BEL)*	(ETB)*						

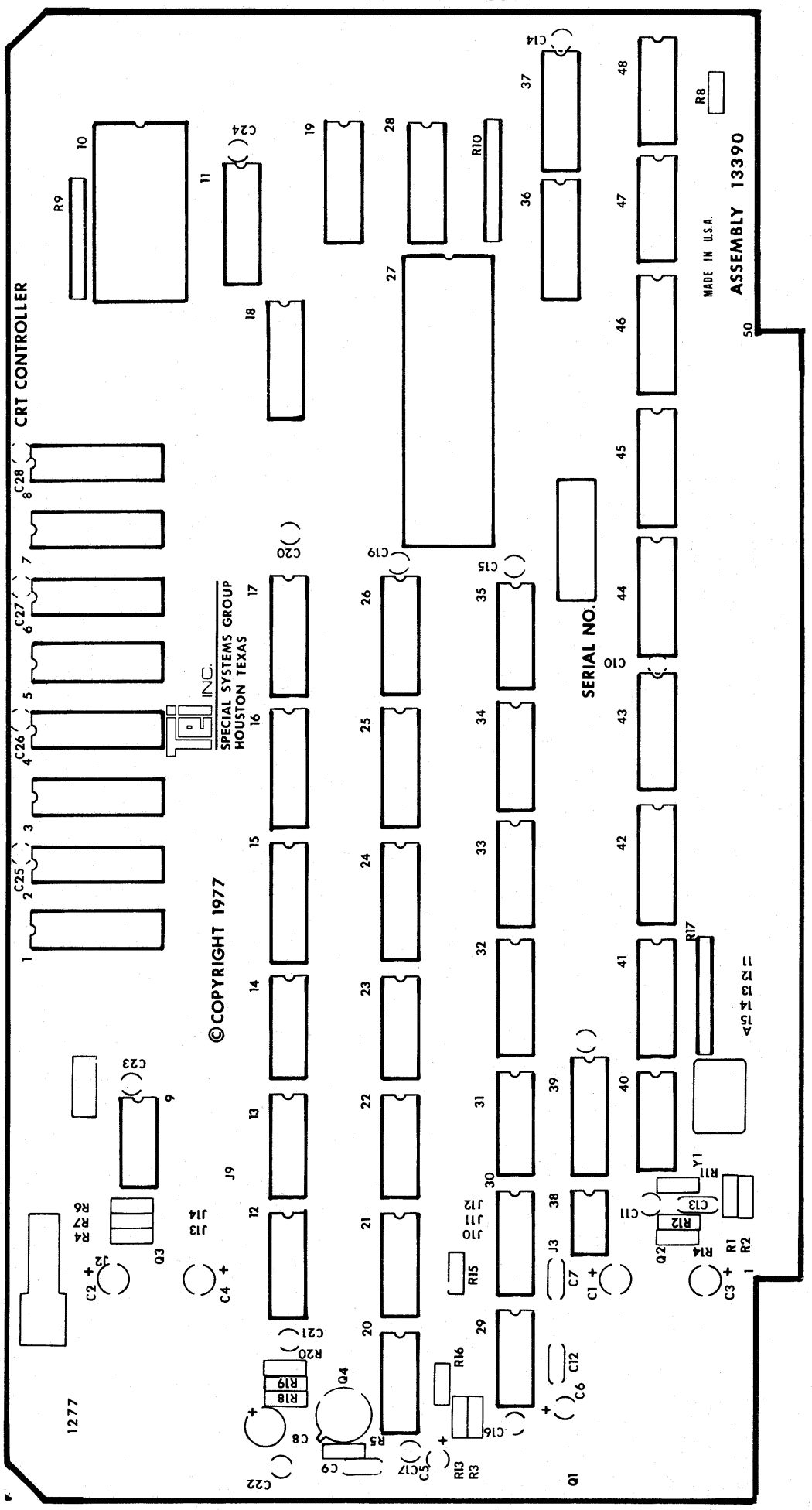
*The letters in parenthesis identify the control code corresponding to the appropriate 35 bit pictorial representation. These representations were obtained from the USASI X 3.2 Code Practice Manual.

A "FILLED IN" DOT REPRESENTS A LOW MEMORY OUTPUT

ASCII INPUT ADDRESS	$B_7B_6B_5$ $A_9A_8A_7$ 000 $O_5O_4O_3O_2O_1$	$A_9A_8A_7$ 001	$A_9A_8A_7$ 010	$A_9A_8A_7$ 011	$A_9A_8A_7$ 100	$A_9A_8A_7$ 101	$A_9A_8A_7$ 110	$A_9A_8A_7$ 111
$B_4B_3B_2B_1$ $A_6A_5A_4A_3$ 1000	(BS)*	(CAN)*						
$A_6A_5A_4A_3$ 1001	(HT)*	(EM)*						
$A_6A_5A_4A_3$ 1010	(LF)*	(SUB)*						
$A_6A_5A_4A_3$ 1011	(VT)*	(ESC)*						
$A_6A_5A_4A_3$ 1100	(FF)*	(FS)*						
$A_6A_5A_4A_3$ 1101	(CR)*	(GS)*						
$A_6A_5A_4A_3$ 1110	(SO)*	(RS)*						
$A_6A_5A_4A_3$ 1111	(SI)*	(US)*						(DEL)*

*The letters in parenthesis identify the control code corresponding to the appropriate 35 bit pictorial representation. These representations were obtained from the USASI X 3.2 Code Practice Manual.

MCS-VCB COMPONENT LAYOUT



TEI INC.

PARTS LIST

MCS-VCB

REF DES	DESCRIPTION	TEI P/N
C1 thru C6, C11	Cap, 10Mf @ 20V	1580-001
C7, C12	Cap, 30Pf	1551-002
C10, C14 thru C28	Cap, .1Mf	1562-002
C13	Cap, 10Pf	1573-006
Q1	Regulator 78M12	3120-006
Q2, Q3	Regulator 7805	3100-003
R1, R2	RES. 270 Ω 1/4 W 2%	4741-283
R3	RES. 9.09K 1/4W 1%	4744-429
R8, R11, R15, R16	RES. 4.7K 1/4W 2%	4741-402
R9, R10, R17	RES Network 4.7K (x8)	4784-001
R12	RES. 47K 1/4W 2%	4741-500
R13	RES. 6.04K 1/4W 1%	4744-412
R14	RES. 27K 1/4W 2%	4741-475
Y1	Crystal 22.225 MHZ	2300-009
Z1 thru Z8	IC Chip 4044-25	3163-006
Z9	IC Chip 7406	3161-028
Z10	IC Chip 6061	3160-019
Z11	IC Chip 74166	3161-033
Z12, Z13, Z34, Z40	IC Chip 7404	3161-016
Z14	IC Chip 7400	3161-018
Z15	IC Chip 74107	3161-013
Z16, Z17	IC Chip 74184	3161-029
Z18	IC Chip 7442	3161-023
Z19, Z28	IC Chip 74175	3161-027
Z20	IC Chip 7474	3161-020
Z21, Z37, Z48	IC Chip 7408	3161-004
Z22	IC Chip 74LS132	3164-019
Z23	IC Chip 74LS02	3164-004
Z24, Z25, Z26	IC Chip 74157	3161-009
Z27	IC Chip 5027	3160-016
Z29, Z30	IC Chip 74121	3161-030
Z31	IC Chip 7432	3161-006
Z32	IC Chip 74LS135	3164-022
Z33	IC Chip 7410	3161-034
Z35	IC Chip 7420	3161-022
Z36, Z47	IC Chip 74125	3161-008
Z38	IC Chip NE555	3100-001
Z39	IC Chip 74163	3161-037
Z41	IC Chip 8131	3160-004
Z42, Z43, Z44	IC Chip 74367	3161-003
Z45, Z46	IC Chip 8216	3162-002

REF DES	DESCRIPTION	TEI P/N
	SEP SYNC VIDEO OPTION	
J10, J14	Jumper (22 Ga Buss)	6009-003
Q4	XISTOR 2N2905A	4863-001
R6	RES 1.0K	4741-337
R7	RES 1.5K	4741-354
R18	RES 75 Ω 1/4 W 1%	4744-229
R19	RES 10 Ω 1/4 W 2%	4741-145
R20	RES 1K 1/4 W 2%	4741-337
	COMPOSITE VIDEO OPTION	
C8	Cap, 10 Mf @ 20V	1580-001
C9	Cap, .IMf	1562-002
J2, J13	Jumper (22GA Buss)	6009-003
R4, R7	RES 100 Ω 1/4 W 2%	4741-241
R5	RES 75 Ω 1/4 W 1%	4744-229
R6	RES 150 Ω 1/4 W 2%	4741-258

IC LIST FOR MCS-VCB

DEVICE NO.	LOGIC
U1-U8	4044-45 4K X 1 MEMORY
U9	7406 OPEN COLLECTOR HEX INVERTER
U10	6061 OR 1K X 8 PROM CHARACTER GENERATOR
U11	74166 8 BIT PARALLEL TO SERIAL SHIFT REGISTER
U12-U13	7404 HEX INVERTER
U14	7400 QUAD NAND GATE
U15	74107 DUAL JK FLIP-FLOP
U16-U17	74184 BINARY TO BCD CONVERTER
U18	7442 3 TO 8 DECODE
U19	74175 QUAD R-S FLIP-FLOP
U20	7474 DUAL R-S FLIP-FLOP
U21	7408 QUAD AND GATE
U22	74132 QUAD SCHMITT TRIGGER INPUT NAND GATE
U23	7402 QUAD NOR
U24-26	74157 MULTIPLEXER
U27	5027 CRT CONTROLLER
U28	74175 QUAD R-S FLIP-FLOP
U29-30	74121 ONE SHOT TIMER
U31	7432 QUAD OR GATE
U32	74135 QUAD EXCLUSIVE OR
U33	7410 TRIPPLE 3 INPUT NAND
U34	7404 HEX INVERTER
U35	7420 DUAL 4 INPUT NAND
U36	74125 TRI-STATE BUSS DRIVER
U37	7408 QUAD AND GATE
U38	555 TIMER
U39	74163 COUNTER
U40	7404 HEX INVERTER
U41	8131 DECODER
U42-44	74367 TRI-STATE BUSS DRIVER
U45-46	8216 BI-DIRECTIONAL BUSS DRIVER
U47	74125 TRI-STATE BUSS DRIVER
U48	7408 QUAD AND GATE

REVISIONS					
ZONE	LTR	EO NO.	DESCRIPTION	DATE	APPROVED
6A	A	1034	CORRECTED Z45 & Z46 LABELING	8-9-78	

COMPOSITE SYNC VIDEO — JUMPER J2 AND J13; REMOVE C4, R19, R12, R20; CHANGE R6 TO 1K; CHANGE R7 TO 1.5K

SEPARATED SYNC VIDEO — JUMPER J16 AND J10; REMOVE C8, C9, R4, R5

VSYNC
HSYNC
RS-172 COMPATIBLE

7812 Q1 +12V — Z27 — C6 10mf 20V, C5 10mf 20V
7805 Q2 +5V — Z20-Z48 — C3 .1mf, C1 10mf 20V
7805 Q3 +5V — Z1-Z19 — C4 10mf 20V, C2 10mf 20V

Z44,43,42 PINS 15&1 TO GND

74367 A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15

74163 Z39 — DOT CLK — Y1 — R1 270Ω — R2 270Ω — C13 10pf

74121 Z30 — R3 9.09K 1% — C7 30pf

Z27-5027

Z16-74184 — Z17-74184

Z25-74157 — Z24-74157 — Z26-74157

4044 — Z1 Z2 Z3 Z4 Z5 Z6 Z7 Z8 — TYPICAL 4044

8131 Z41 — R17 4.7K X5 RES — A11 ALL OPEN FOR F800, A12, A13, A14, A15

7432 R/W — SMER — PBBN — PAM — MWRITE — READ — WRITE

7420 Z27 PIN 3 — SINP — SOUT — PWR

74LS135

8216 Z45 — 8216 Z46

7408 Z1-11 Z2-11 Z3-11 Z4-11 Z5-11 Z6-11 Z7-11 Z8-11 — Z37 Z37 Z37 Z37 Z48 Z48 Z48 Z48

74125 Z1-7 Z2-7 Z3-7 Z4-7 Z5-7 Z6-7 Z7-7 Z8-7 — R10 4.7K X8

7410 — 74LS32 — 74LS02 — 74LS35 — 74LS135

CUT TRACE AND JUMPER J9 FOR BLOCK CURSOR

CUT TRACE FOR NON BLINKING CURSOR D5

R11 4.7K — R15 4.7K — R16 4.7K

Z29 74121 — R13 6.04K 1% — R14 47K — RM 27K — Z38 555 — C11 10mf 20V — C12 .33pf

Z18 7442

7475 Z19 — 7442 Z28

Z10 6061

Z11-74166 — R9 4.7K PULLUP RESISTOR ON EACH LINE — DOT CLK LOAD CLK

7474 Z20 — 74107 Z15

R4 100Ω — R5 75Ω — C8 100mf — C9 1mf — COMPOSITE VIDEO 2010B

R20 1K — R19 10Ω — Q4 2N2905 — R18 75Ω ± 1%

R6 150Ω — R7 100Ω

PSYNC

NOTES:

QTY	PART NUMBER	DESCRIPTION	MANUFACTURER	CODE IDENT	REF DES	ITEM

PARTS LIST

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.X ± .06
.XX ± .02
.XXX ± .010
ANGULAR ± .5 DEG

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

MATERIAL

CONTRACT NO.

SIGNATURES	DATE
DR	11-17-77
DES	
CHK E. McCain	8-8-78
ENGR	9-9-78
APP	
APP	

NEXT ASSY | USED ON

APPLICATION

TEXAS ELECTRONIC INSTRUMENTS INC
HOUSTON, TEXAS

MCS-VCB
(CRT CONTROLLER)

SIZE	CODE IDENT NO.	DWG NO.	REV
D	33179	13388	A

SCALE | REL EO NO. | SHEET 1 OF 1

DRAWING 13388 REV A

8-12

TEI INC.

5075 S. Loop East
Houston, Texas 77033

713-738-2300
TWX: 1-910-881-3639

SECTION IX
MINI-FLOPPY DISK DRIVE
(400 SERIES)
TEI INC.

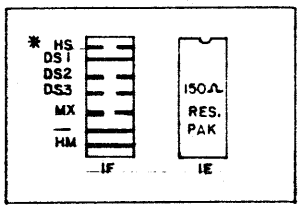
P/N 13686-9

SECTION IX
MINI-FLOPPY DISK DRIVE

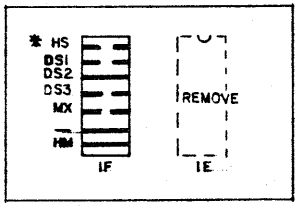
		PAGE
A.	TEI, INC. MINI-FLOPPY SELECT OPTIONS	9-2
B.	SA 400 DRIVE	
1.	INTRODUCTION	9-3
2.	FUNCTIONAL CHARACTERISTICS	9-5
3.	FUNCTIONAL OPERATIONS	9-7
4.	ELECTRICAL INTERFACE	9-13
5.	PHYSICAL INTERFACE	9-19
6.	OPERATING PROCEDURES	9-21
7.	PCB COMPONENT LOCATIONS	9-23
8.	LOGIC DIAGRAMS	9-26
9.	PARTS LIST	9-31

REVISIONS					
ZONE	LTR	EO NO.	DESCRIPTION	DATE	APPROVED

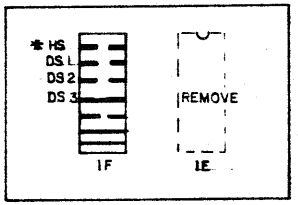
MINI DRIVE A



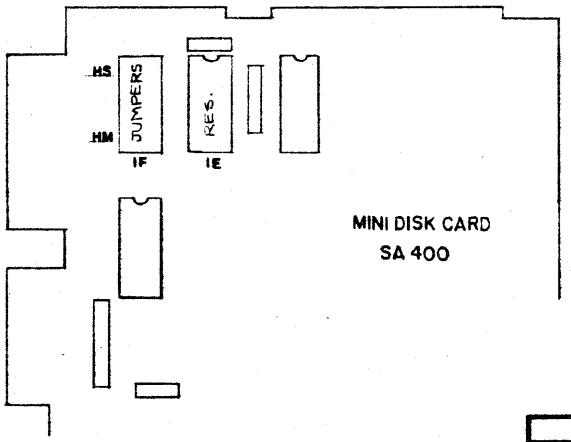
MINI DRIVE B



MINI DRIVE C



* NOTE: SHUNT BLOCK IS ONLY A 6 POSITION JUMPER BLOCK. SHIFT DOWN 1 HOLE IN SOCKET



NOTES:

QTY	PART NUMBER	DESCRIPTION	MANUFACTURER	CODE IDENT	REF DES	ITEM
PARTS LIST						

NEXT ASSY	USED ON
APPLICATION	

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.X ± .06
.XX ± .02
.XXX ± .010
ANGULAR ± .5 DEG

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

MATERIAL

CONTRACT NO.

SIGNATURES	DATE
DR	5/12/17
DES	
CHK	
ENGR	
APP	
APP	

TEXAS ELECTRONIC INSTRUMENTS, INC
HOUSTON, TEXAS

SHUGART SA400
MINI FLOPPY DRIVE
SELECT OPTIONS

SIZE	CODE IDENT NO.	DWG NO.	REV
C	33179	13554	

SCALE | REL EO NO. | SHEET 1 OF 1

1.0 INTRODUCTION

The SA400 minifloppy™drive offers the system designer the random access storage capability of floppy disk drives in a package the size of most cassette tape units. It also provides superior data integrity and faster throughput of data when compared with cassette drives.

The SA400 is based on the proven floppy disk drive technology of the Shugart SA800 drive. It features a unique new direct drive stepping motor actuator, utilizing a spiral cam with a v-groove positive detent which assures precise location of the read/write head on a track. The drive employs the same proprietary glass bonded ferrite/ceramic read/write head as the SA800 uses. AC power requirements have been eliminated through the use of a DC servo-controlled spindle drive motor. The drive is also equipped with an interface which allows upward expansion of the units within the system and future system enhancements with the large floppy drive.

Applications for the minifloppy drive include word processing and text editing systems; mini and micro computer program storage; power typing systems; "intelligent" desktop calculators and the microcomputer hobby market.

The SA104/105/107 minidiskette™ media used with the SA400 is similar to the standard flexible disk, only smaller. It is available for soft (SA104) or hard (SA105/107) sectored formats. The minidiskette diameter is 5.125 inches (130.2 mm) and the jacket is a square 5.25 inches (133.4 mm).

1.1 Specification Summary

1.1.1 Performance Specifications

Capacity		
Unformatted		
per disk	109.4K bytes	
per track	3125 bytes	
Formatted (Reference Section 7.0)		
	Soft Sectoring	**Hard Sectoring**
per disk	80.6K bytes	72.03K bytes
per track	2304 bytes	2058 bytes
per sector	128 bytes	128 bytes
sectors per track	18	16
Transfer Rate	125.0K bits/sec.	
Latency (average)	100 ms	
Access Time		
track to track	40 ms	
average	463 ms	
settling time	10 ms	
Head Load Time	75 ms	
Disc Motor Start Time	1 sec.	

1.1.2 Functional Specifications

Rotational Speed	300 RPM
Recording Density (inside track)	2581 BPI
Flux Density	5162 FCI
Track Density	48 TPI
Tracks	35
Inside Track Radius	1.542 in. (3.916 cm)
Outside Track Radius	2.250 in. (5.715 cm)
Index	1
Encoding Method	FM
Media Requirements	SA 105 or SA107 minidiskette (Hard Sectored) SA104 minidiskette (Soft Sectored)

1.1.3 Physical Specifications

Environmental Limits:

Ambient Temperature =

Operating	**Shipping**	**Storage**
40°F to 115°F (4°C to 46°C)	-40°F to 144°F (-40°C to 62°C)	-8°F to 117°F (-22°C to 47°C)

Relative Humidity =

20% to 80%	1% to 95%	1% to 95%

Max. Wet. Bulb =

78°F (25°C) No Condensation

DC Voltage Requirements:

+12 VDC ± 5%	0.9 amp (typical)	1.8 amp (maximum)
+5 VDC ± 5%	0.5 amp (typical)	0.7 amp (maximum)

Mechanical Dimensions:

Width	5.75 in. (14.60 cm.)
Height	3.25 in. (8.25 cm.)
Depth	8.00 in. (20.32 cm.)
Weight	3 lbs. (1.36 kg.)

Power Dissipation =

15 watts (51 BTU/Hr) Operating (typical)

7.5 watts (26 BTU/Hr) Standby (typical)

1.1.4 Reliability Specifications

*MTBF (Mean Time Between Failures)	8,000 Power on Hours (Typical Usage)
PM (Preventive Maintenance)	Not Required
MTTR (Mean Time to Repair)	30 Minutes
Error Rates	
Soft Errors	1 per 10^8 bits read
Hard Errors	1 per 10^{11} bits read
Seek Errors	1 per 10^6 seeks
Component Design Life	5 years
Media Life	3.0×10^6 passes per track

*MTBF assumes duty cycle of spindle drive motor to be 25% of POH.

2.0 FUNCTIONAL CHARACTERISTICS

2.1 General Operation

The SA400 minidiskette Storage Drive consists of read/write, control and drive motor electronics, drive mechanism, read/write head, track positioning mechanism, and removable minidiskette. These components perform the following functions:

1. Interpret and generate control signals.
2. Move the read/write head to the desired track.
3. Read and write data.
4. Control drive motor speed.

The interface signals and their relationship to the internal functions are shown in figure 2.

The head positioning actuator positions the read/write head to the desired track on the minidiskette. The head load actuator loads the minidiskette against the read/write head and data may then be recorded or read.

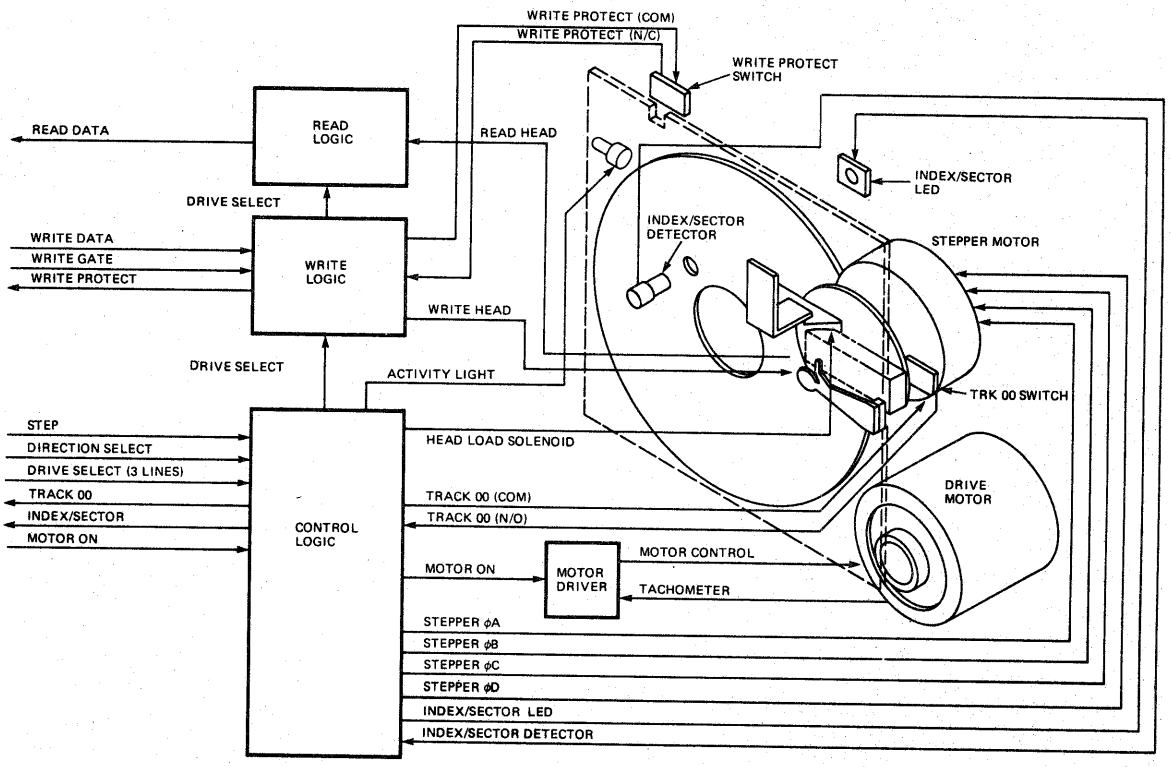


FIGURE 2. SA400 FUNCTIONAL DIAGRAM

2.2 Read/Write and Control Electronics

The electronics are packaged on two PCB's. The PCB's contain:

1. Index/Sector detector.
2. R/W head position actuator drivers.
3. R/W head load actuator driver.
4. Write current drivers.
5. Read amplifier and transition detectors.
6. Write protect detector.
7. Drive select circuits.
8. Drive motor control circuits.

2.3 Drive Mechanism

The minifloppy drive motor operates on 12 VDC and rotates the spindle at 300 rpm through a belt-drive system. The speed of the motor is controlled by a feed back from a tachometer internal to the motor. A registration hub, centered on the face of the spindle, positions the minidiskette. A hub clamp that moves in conjunction with the door closure mechanism centers and clamps the minidiskette onto the spindle hub.

2.4 R/W Head Positioning Mechanism

An electrical stepping motor and a face cam positions the read/write head. The stepping motor rotates the cam clockwise or counterclockwise with two step increments per track. The using system increments the stepper motor to the desired track by selecting the proper direction and issuing one step pulse per track. The drive control electronics issues the second step pulse needed per track.

2.5 Read/Write Head

The SA400 R/W head is a single element glass bonded ferrite/ceramic head with straddle erase elements to provide erased areas between data tracks. Thus normal interchange tolerances between media and drives will not degrade the signal to noise ratio and insures minidiskette interchangeability.

The R/W head is mounted on a carriage assembly which moves on rails and is positioned by the cam. The minidiskette is held in a plane perpendicular to the R/W head by a platen located on the base casting. This precise registration assures perfect compliance with the R/W head. The minidiskette is loaded against the head with a load pad actuated by the head load solenoid.

The R/W head is in direct contact with the minidiskette. The head surface has been designed to obtain maximum signal transfer to and from the magnetic surface of the minidiskette with minimum head/minidiskette wear.

2.6 Recording Format

The format of the data recorded on the disk is totally a function of the host system, and can be designed around the users application to take maximum advantage of the total available bits that can be written on any one track.

For a detailed discussion of various recording formats, reference section 7.0.

3.0 FUNCTIONAL OPERATIONS

This section of the manual defines the functional as well as the timing relationships of the operations for the SA400.

3.1 Power Sequencing

Applying DC power to the SA400 can be done in any sequence; however, during power up, the Write Gate line must be held inactive or at a high level. This will prevent possible "glitching" of the media. After application of DC power, a 100 ms delay should be introduced before any operation is performed. Also, after powering on, initial position of the R/W head with respect to the data tracks on the media is indeterminant. In order to assure proper positioning of the R/W head after powering on, a Step Out operation should be performed until the Track 00 line becomes active (Recalibrate).

3.2 Drive Selection

Drive Selection occurs when the Drive Select line is activated. Under normal operation, the Drive Select line will load the R/W head against the minidiskette enabling contact of the R/W with the media and will also light a LED on the front plate.

3.3 Motor On

In order for the host system to read or write data the DC drive motor must be turned on. This is accomplished by activating the line -Motor On. A one (1) second delay must be introduced after activating this line to allow the motor to come up to speed before reading or writing can be accomplished.

The motor must be turned off by the host system by deactivating the Motor On line. This should be done if the drive has not received a new command within two (2) seconds (10 revolutions of diskette) after completing the execution of a command. This will insure maximum motor and media life.

3.4 Track Accessing

Seeking the R/W head from one track to another is accomplished by:

1. Activating the Drive Select line.
2. Selecting the desired direction utilizing the Direction Select line.
3. Write Gate being inactive.
4. Pulsing the Step line.

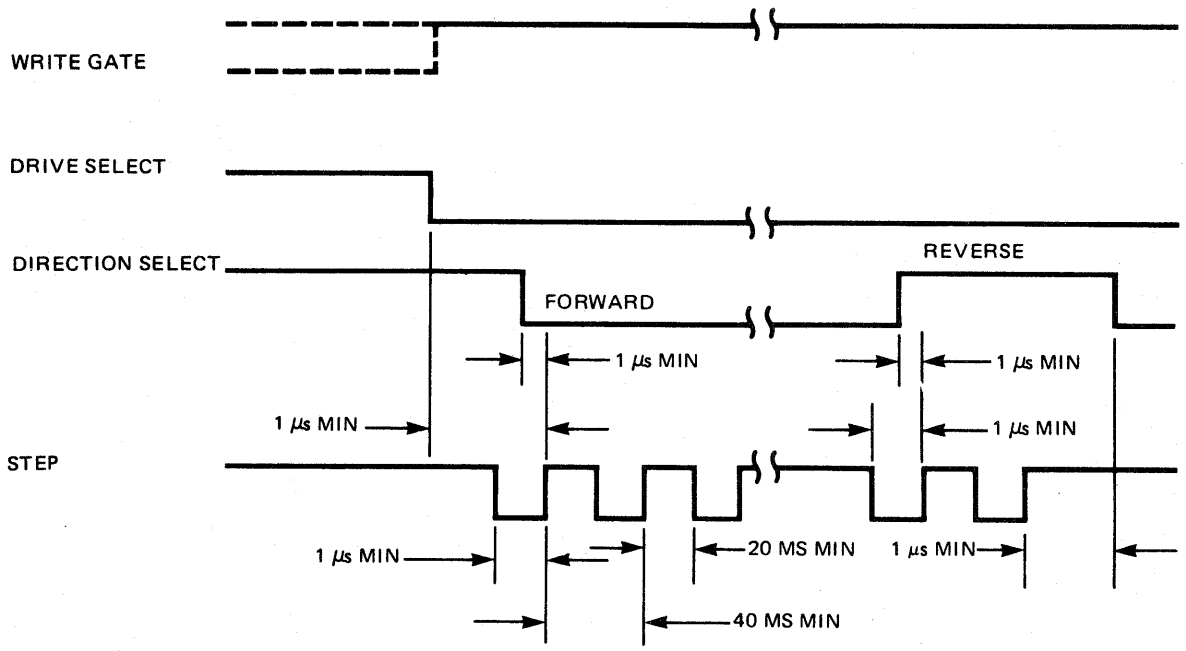


FIGURE 3. TRACK ACCESS TIMING

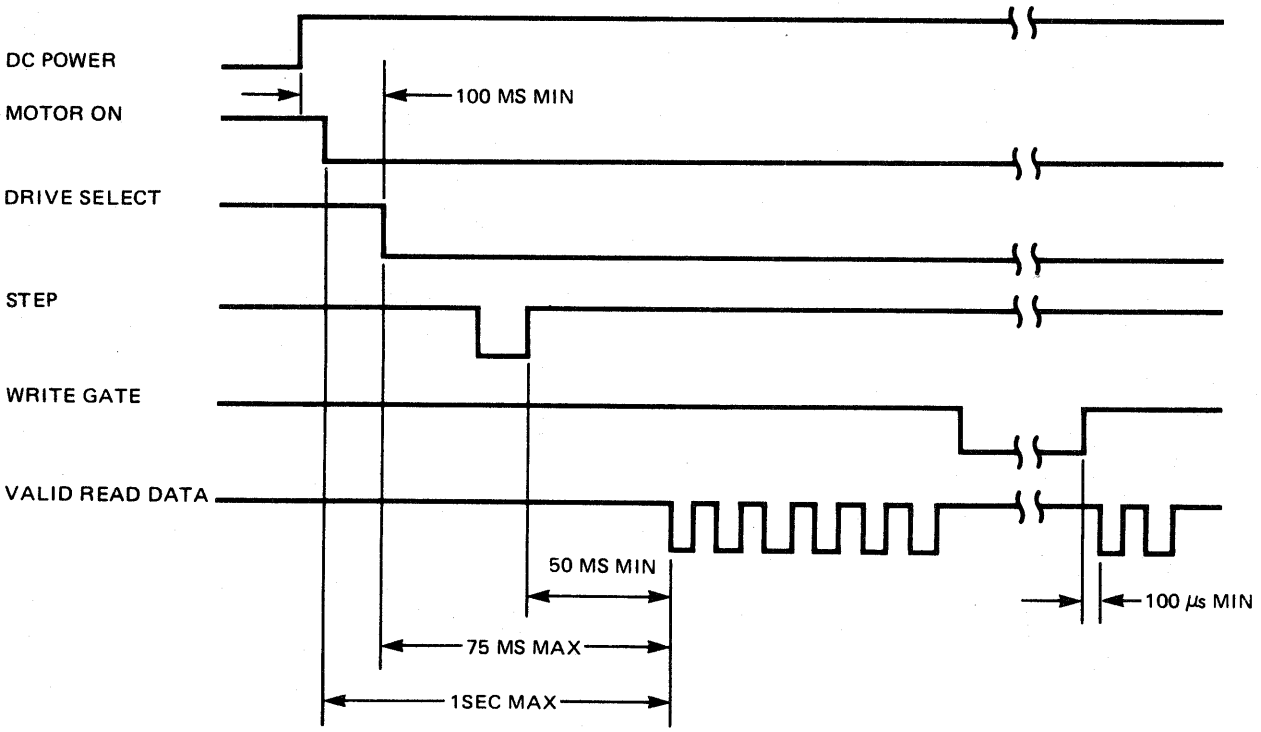


FIGURE 4. READ INITIATE TIMING

Multiple track accessing is accomplished by repeatedly pulsing the Step line until the desired track has been reached. Each pulse on the Step line will cause the R/W head to move one track either in or out depending on the Direction Select line. Head movement and direction latching is initiated on the trailing edge of the Step pulse.

During a Recalibrate (Step to Track 00), the worst case number of step pulses required is 58. The worst case occurs when the carriage is positioned IN beyond track 34 and the carriage comes out of the spiral cam groove. In this case, it can take up to 24 steps for the carriage to pick up the groove in the cam and then another 34 steps to reach track 00.

3.4.1 Step Out

With the Direction Select line at a plus logic level (2.5V to 5.25V) a pulse on the Step line will cause the R/W head to move one track away from the center of the disk. The pulse(s) applied to the Step line and the Direction Select line must have the timing characteristics shown in Figure 3.

3.4.2 Step In

With the Direction Select line at a minus logic level (0V to .4V), a pulse on the Step line will cause the R/W head to move one track closer to the center of the disk. The pulse(s) applied to the Step line must have the timing characteristics shown in figure 3.

3.5 Read Operation

Reading data from the SA400 minifloppy drive is accomplished by:

a. Activating Drive Select line.

b. Write Gate being inactive.

The timing relationships required to initiate a read sequence are shown in figure 4. These timing specifications are required in order to guarantee that the R/W head position has stabilized prior to reading.

The timing of Read Data is shown in figure 5.

3.6 Write Operation

Writing data to the SA400 is accomplished by:

a. Activating the Drive Select line.

b. Activating the Write Gate line.

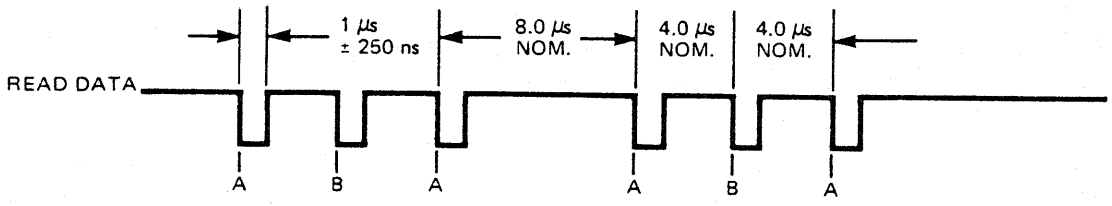
c. Pulsing the Write Data line with the data to be written.

The timing relationships required to initiate a write data sequence are shown in Figure 6. These timing specifications are required in order to guarantee that the R/W head position has stabilized prior to writing.

The timing specifications for the Write Data pulses are shown in figure 7.

3.7 Sequence of Events

The timing diagram shown in figure 8 shows the necessary sequence of events with associated timing restrictions for proper operation.



A = LEADING EDGE OF BIT MAY BE ± 800 ns FROM ITS NOMINAL POSITION.
B = LEADING EDGE OF BIT MAY BE ± 400 ns FROM ITS NOMINAL POSITION.

FIGURE 5. READ SIGNAL TIMING

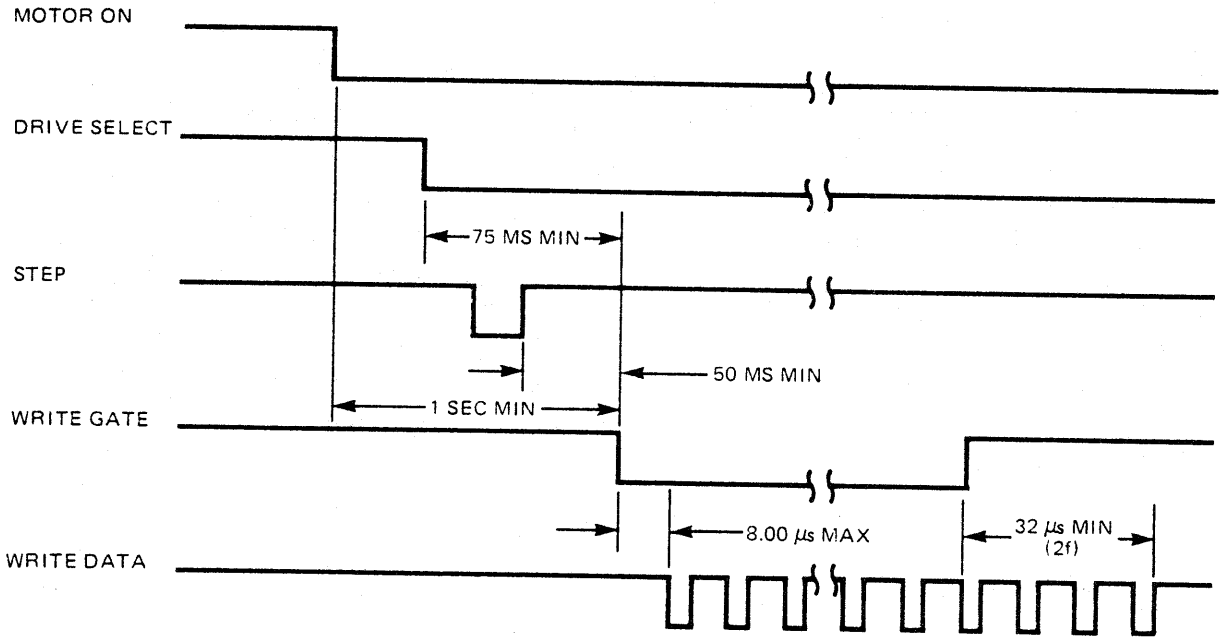


FIGURE 6. WRITE INITIATE TIMING

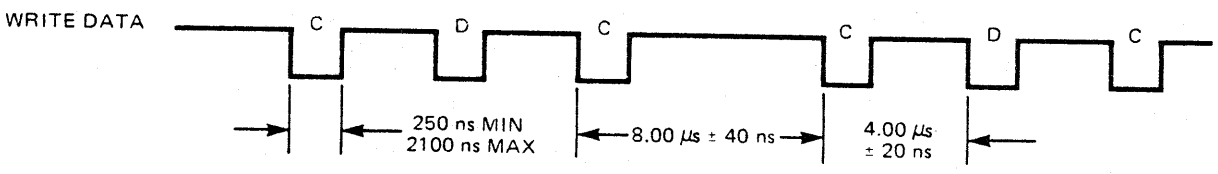


FIGURE 7. WRITE DATA TIMING

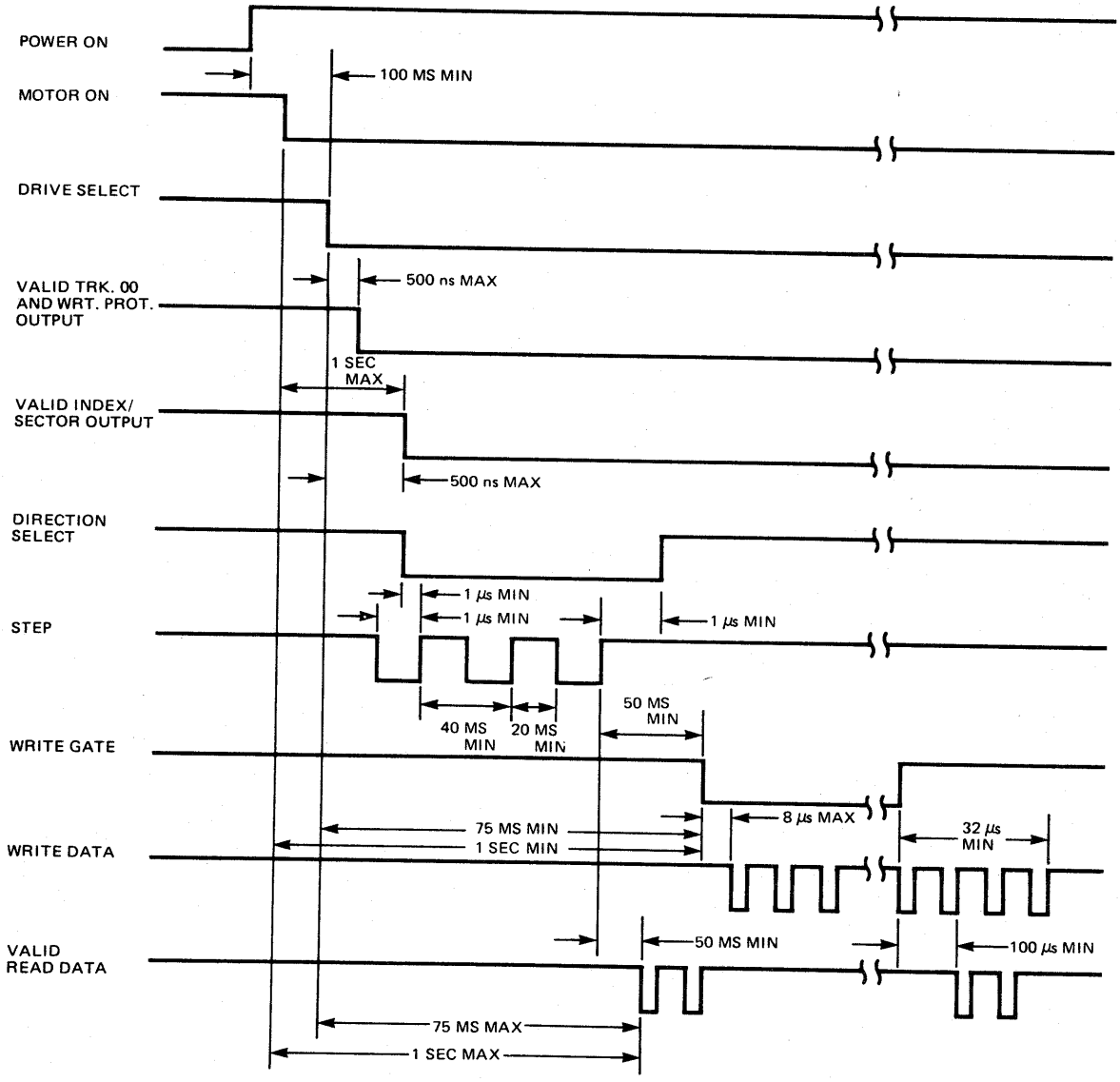


FIGURE 8. GENERAL CONTROL AND DATA TIMING REQUIREMENTS

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4.0 ELECTRICAL INTERFACE

The interface of the SA400 minidiskette drive can be divided into two categories:

1. Signal

2. Power

The following sections provide the electrical definition for each line.

Reference figure 9 for all interface connections.

4.1 Signal Interface

The signal interface consists of two categories:

1. Control

2. Data transfer

All lines in the signal interface are digital in nature and eitner provide signals to the drive (input), or provide signals to the host (output), via interface connector P1/J1.

4.1.1 Input Lines

The input signals are of 3 types, those intended to be multiplexed in a multiple drive system, those which will perform the multiplexing and Motor Control.

The input signals to be multiplexed are:

1. Direction Select

2. Step

3. Write Data

4. Write Gate

The input signals which are intended to do the multiplexing are:

1. Drive Select 1

2. Drive Select 2

3. Drive Select 3

The input lines have the following electrical specifications. Reference Figure 10 for the recommended circuit.

True = Logical zero = Vin ±0.0V to +0.4V
@ Iin = 40 ma (max)

False = Logical one = Vin +2.5V to +5.25V
@ Iin = 0 ma (open)

Input Impedance = 150 ohms

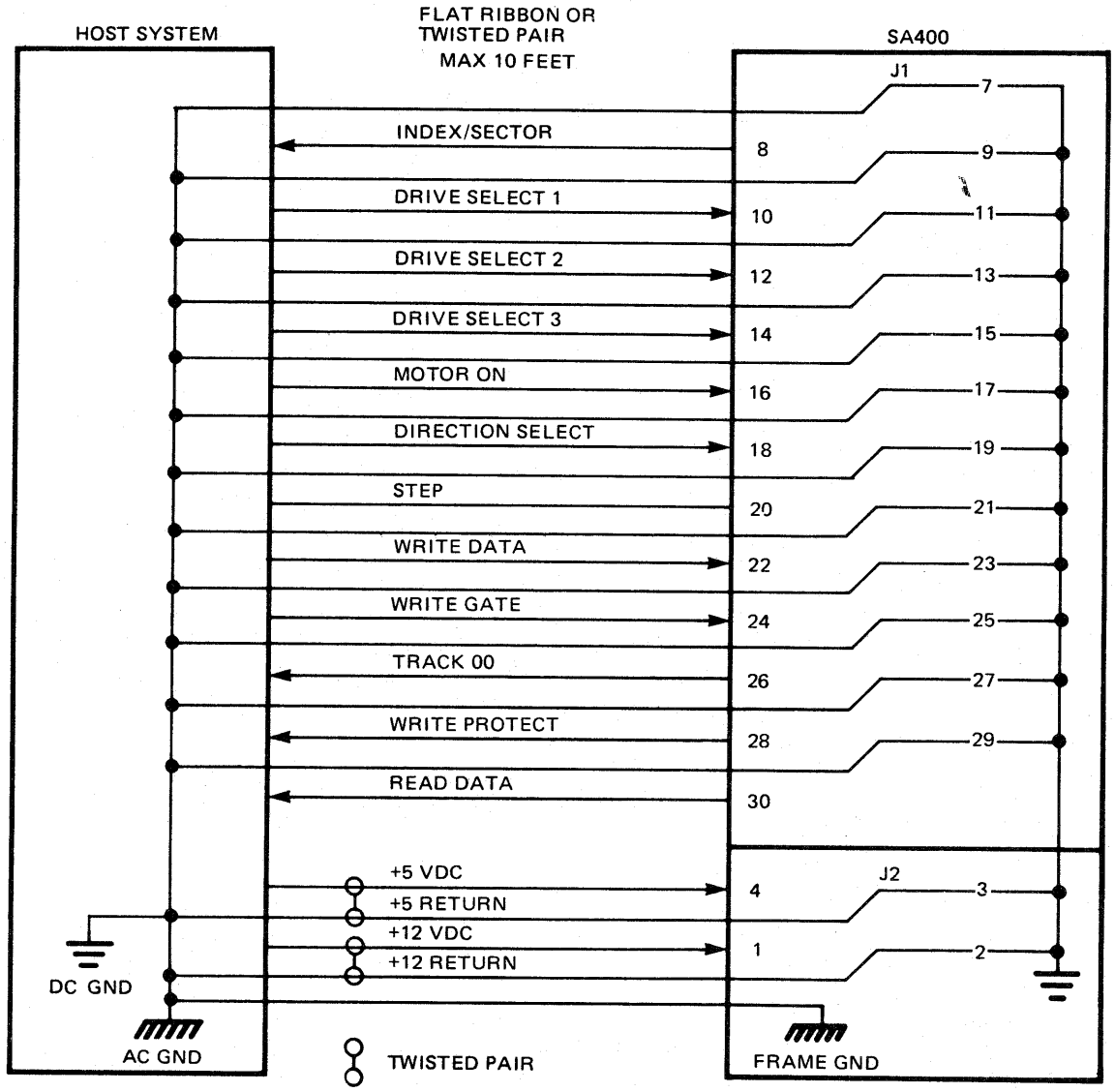

FIGURE 9. INTERFACE CONNECTIONS

4.1.1.1 Input Line Terminations

The SA400 has been provided with the capability of terminating the five input lines listed below.

1. Motor On
2. Direction Select
3. Step
4. Write Data
5. Write Gate

These lines are terminated through a 150 ohm resistor pack installed in a dip socket located at IC location 1E.

In a single drive system this resistor pack should be kept in place to provide the proper terminations.

In a multiple drive system (Program Shunt position "MX" open) only the last drive on the interface is to be terminated. All other drives on the interface must have the resistor pack removed. External terminations may also be used, then the user must provide the terminations beyond the last drive and each of the five lines must be terminated to +5VDC through a 150 ohm ¼ watt resistor.

4.1.1.2 Drive Select 1-3

The SA400 as shipped from the factory is configured to operate in a single drive system. It can be easily modified by the user to operate with other drives in a multiplexed multiple drive system. The user can activate the multiplex option by cutting the "MX" position of the programmable shunt located in IC location 1F. This will allow the multiplexing of the I/O lines.

In a single drive system (program shunt position "MX" shorted), with program shunt position "HS" shorted, Drive Select when activated to a logical zero level, will load the R/W head against the diskette enabling contact of the R/W head against the media. Since "MX" is shorted, the I/O lines are always enabled.

In a multiple drive system (program shunt position "MX" open) the three input lines (Drive Select 1, Drive Select 2 and Drive Select 3) are provided so that the using system may select which drive on the interface is to be used. In this mode of operation only the drive with its Drive Select line active will respond to the input lines and gate the output lines. In addition, the selected drive will load its R/W head if program shunt position "HS" is shorted.

The program shunt, IC location 1F, positions "DS1", "DS2" and "DS3", are to be used to select which Drive Select line will active the I/O lines for a unique drive. As an example, if the user wants the first drive on the interface to be address 1, he must cut program shunt positions "DS2" and "DS3", and leave "DS1" intact.

The program shunt is AMP part number 435704-6. The shunt positions can be cut using AMP's tool part number 435705. The shunt is installed in a dip socket and at the user's option be removed and be replaced by a dip switch (AMP P/N 435626-4). The user may also choose to have the program shunts pre-programed and/or color coded by AMP. For this service contact your local AMP representative.

4.1.1.3 Motor On

This input when activated to a logical zero level will turn on the drive motor allowing reading or writing on the drive. A one (1) second delay after activating this line must be allowed before reading or writing. This line should be deactivated, for maximum motor life, if no commands have been issued to the drives within two seconds (10 revolutions of the media) after completion of a previous command.

As discussed in section 4.1.1.2, when program shunt position "HS" is shorted the R/W head will load when the Drive Select line is activated. A user selectable option is available where by the R/W head will load when the Motor On line is activated. This is accomplished by moving the program shunt over one position in its socket so position "HM" is shorted and position "HS" is open. With position "HM" shorted, the R/W head will load when the Motor On line is activated to a logical zero level.

4.1.1.4 Direction Select

This interface line is a control signal which defines direction of motion the R/W head will take when the Step line is pulsed. An open circuit or logical one defines the direction as "out" and if a pulse is applied to the Step line the R/W head will move away from the center of the disk. Conversely, if this input is shorted to ground or a logical zero level, the direction of motion is defined as "in" and if a pulse is applied to the step line, the R/W head will move towards the center of the disk.

4.1.1.5 Step

This interface line is a control signal which causes the R/W head to move with the direction of motion as defined by the Direction Select line.

The access motion is initiated on each logical zero to logical one transition, or the trailing edge of the signal pulse. Any change in the Direction Select line must be made at least 1μs before the trailing edge of the Step pulse. Direction Select logic level must be maintained 1μs after trailing edge of Step pulse. Refer to figure 3 for these timings.

4.1.1.6 Write Gate

The active state of this signal, or logical zero, enables Write Data to be written on the diskette. The inactive state, or logical one, enables the read data logic and stepper logic. Refer to figure 6 for timings.

4.1.1.7 Write Data (FM)

This interface line provides the data to be written on the diskette. Each transition from a logical one level to a logical zero level, will cause the current through the R/W head to be reversed thereby writing a data bit. This line is enabled by Write Gate being active. Refer to figure 7 for timings.

4.1.2 Output Lines

The output control lines have the following electrical specifications. Refer to figure 10 for the recommended circuit.

True = Logical Zero = Vout + 0.0V to + 0.4V @ Iout = 48 ma (max)

False = Logical On = Vout + 2.5V to 5.25V (open collector @ Iout = 250 μa max)

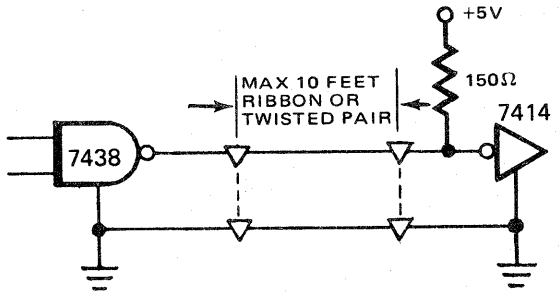

FIGURE 10. INTERFACE SIGNAL DRIVER/RECEIVER

4.1.2.1 Track 00

The active or logical zero state of this interface signal indicates when the drive's R/W head is positioned at track zero (the outermost track) and the access circuitry is driving current through phase "A" of the stepper motor. This signal is at a logical one level, or inactive state, when the

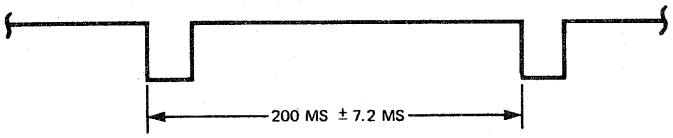

FIGURE 11. INDEX TIMING (SA104 MEDIA)

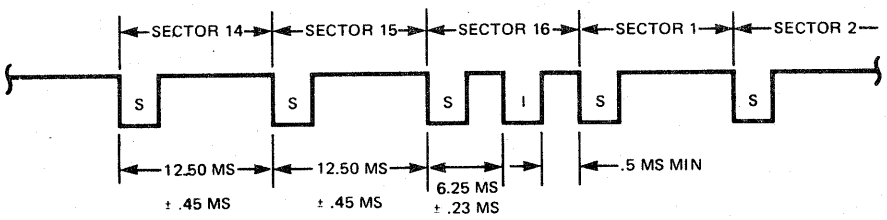

FIGURE 12. INDEX/SECTOR TIMING (SA105 MEDIA)

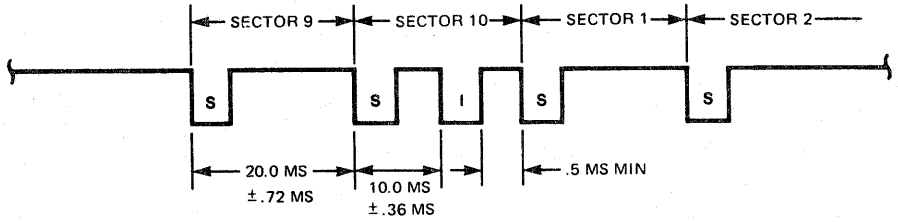

FIGURE 12.1 INDEX/SECTOR TIMING (SA107 MEDIA)

drive's R/W head is not at track zero. When the drive's R/W head is at track zero and an additional step out pulse is issued to the drive, a mechanical stop will keep the R/W head at track zero but the Track 00 signal will go inactive. This is because the stepper motor will go to phase "C" and not phase "A". One more step out pulse will put the stepper motor back into phase "A" and the Track 00 signal will go active again.

4.1.2.2 Index/Sector

This interface signal is provided by the drive each time an index or sector hole is sensed at the Index/Sector photo detector. Normally, this signal is at a logical one level and makes the transition to the logical zero level each time a hole is sensed.

When using SA104 media (Soft Sectored), there will be one pulse on this interface signal per revolution of the diskette (200 ms). This pulse indicates the physical beginning of a track. Reference figure 11 for the timing.

When using SA105 or SA107 media (Hard Sectored), there will be 17 or 11 pulses on this interface line per revolution (200 ms). To indicate the beginning of a track, once per revolution there is one index transition between 16 or 10 equally spaced sector transitions. The timing for this signal is in figure 12. For recommended Index/Sector separator circuit, reference section 8.4.

When using the Index/Sector signal, look for an edge or transition rather than a level for determining its status. With no diskette inserted, this signal remains active or at a logical zero level which is an erroneous status.

4.1.2.3 Read Data

This interface line provides the "raw data" (clock and data together) as detected by the drive electronics. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference figure 5 for the timing and bit shift tolerance within normal media variations.

4.1.2.4 Write Protect

This interface signal is provided by the drive to give the user an indication when a Write Protected Diskette is installed. The signal is logical zero level when it is protected. Under normal operation, the drive will inhibit writing with a protected diskette installed in addition to notifying the interface.

4.2 Power Interface

The SA400 requires only DC power for operation. DC power to the drive is provided via P2/J2 located on the non-component side of the PCB near the spindle drive motor. The two DC voltages, their specifications and their P2/J2 pin designators are outlined below. The specifications outlined on current requirements are for one drive. For multiple drive systems the current requirements are a multiple of the maximum current times the number of drives in the system.

4.2.1 Frame Ground

It is important that the drive be frame grounded to the host systems AC or frame ground. Failure to do so may result in drive noise susceptibility. Reference section 5.3 for the procedure.

P2 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (p to p)
1	+12 VDC	± 0.6 VDC	*1.80A MAX .90A TYP	100 mV max allowable
2	+12 Return			
3	+ 5 Return			
4	+ 5 VDC	± 0.25 VDC	.70A MAX .50A TYP	50 mV max allowable

*The 12 VDC current is composed of three components; head load current, diskette drive motor current, PCB functions and stepper motor. Each of these components has the following contribution to the 12 VDC current requirements.

1. PCB functions and stepper motor (Drive "Standby" current): 0.4A TYP; 0.5A MAX
2. Head Load (Drive Selected): 0.15A TYP; 0.2A MAX
3. Drive Motor: Start (for 1 sec. max.)–1.0A TYP; 1.1A MAX
   Running–0.35A TYP; 1.1A MAX (Motor Stalled)

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5.0 PHYSICAL INTERFACE

The electrical interface between the SA400 and the host system is via two connectors. The first connector, J1, provides the signal interface and the second connector, J2, provides the DC power.

This section describes the physical connectors used on the drive and the recommended connectors to be used with them. Refer to figure 15 for connector locations.

5.1 J1/P1 Connector

Connection to J1 is through a 34 pin PCB edge card connector. The dimensions for this connector are shown in figure 13. The pins are numbered 1 through 34 with the even numbered pins on the component side of the PCB and the odd numbered pins on the non-component side. Pin 2 is located on the end of the PCB connector closest to the corner and is labeled 2. A key slot is provided between pins 4 and 6 for optional connector keying.

The recommended connectors for P1 are tabulated below.

TYPE OF CABLE	MANUFACTURER	CONNECTOR P/N	CONTACT P/N
Twisted Pair, #26	AMP	583717-5	1-583616-1
Flat Cable	3M "Scotchflex"	3463-0001	NA

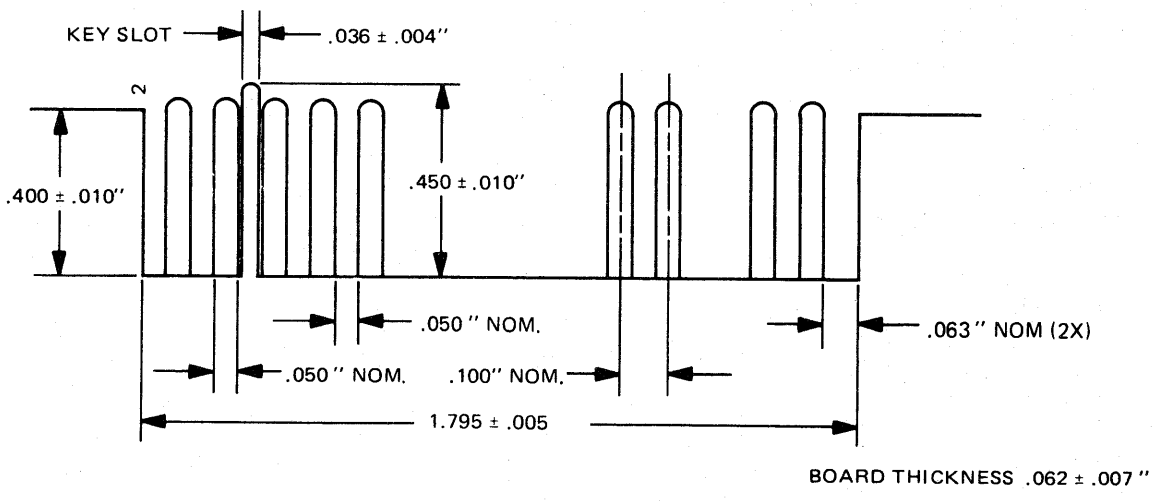


FIGURE 13. J1 CONNECTOR DIMENSIONS

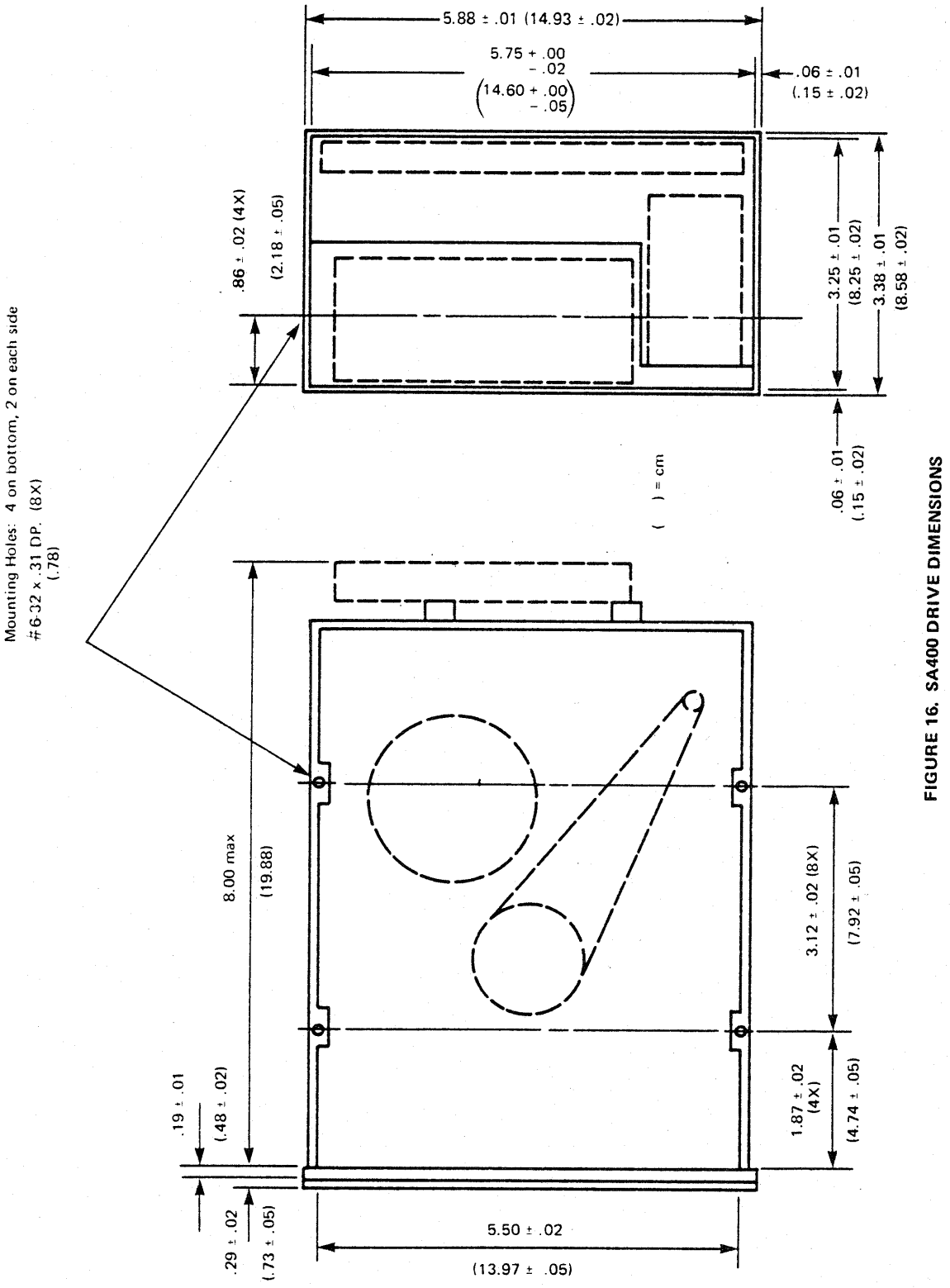


FIGURE 16. SA400 DRIVE DIMENSIONS

9.0 OPERATION PROCEDURES

The SA400 was designed for ease of operator use to facilitate a wide range of operator orientated applications. The following section is a guide for the handling procedures on the minidiskette and minifloppy drive.

9.1 Minidiskette Loading

Figure 37 shows the proper method of loading a minidiskette in the SA400. To load the diskette, open the door on the front panel, insert the diskette with label towards the door handle and close handle. A mechanical interlock prevents door closure without proper media insertion, thus eliminating media damage.

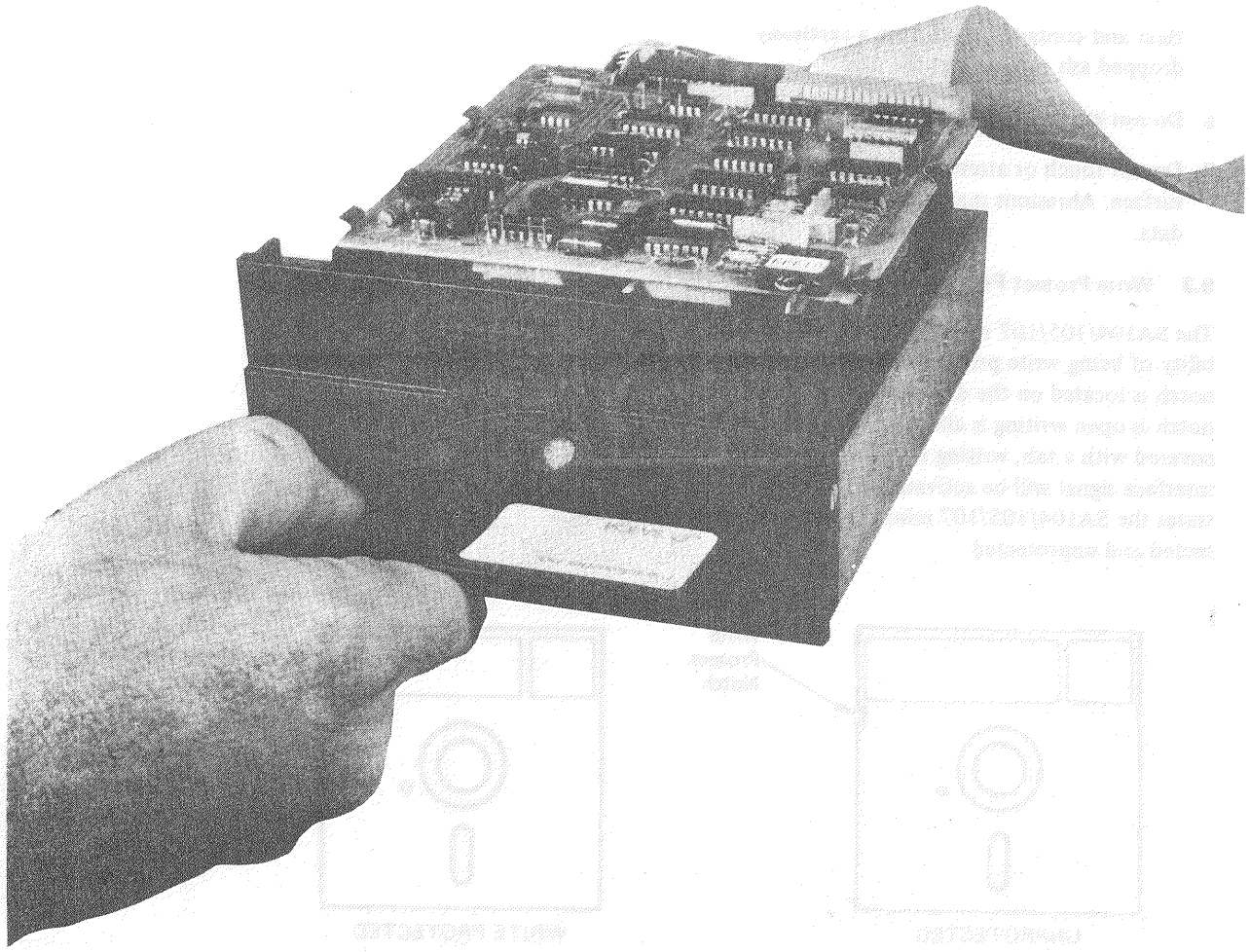


FIGURE 37. LOADING SA400

9.2 Minidiskette Handling

To protect the diskette, the same care and handling procedures specified for computer magnetic tape apply. These precautionary procedures are as follows:

1. Return the diskette to its storage envelope whenever it is removed from file.
2. Keep cartridges away from magnetic fields and from ferromagnetic materials which might become magnetized. Strong magnetic fields can distort recorded data on the disk.
3. Replace storage envelopes when they become worn, cracked or distorted. Envelopes are designed to protect the disk.
4. Do not write on the plastic jacket with a lead pencil or ball-point pen. Use a felt tip pen.
5. Heat and contamination from a carelessly dropped ash can damage the disk.
6. Do not expose diskette to heat or sunlight.
7. Do not touch or attempt to clean the disk surface. Abrasions may cause loss of stored data.

9.3 Write Protect Feature

The SA104/105/107 minidiskettes have the capability of being write protected. A write protect notch is located on the diskette jacket. When the notch is open writing is allowed. When the notch is covered with a tab, writing is inhibited and the interface signal will be activated. Figure 38 illustrates the SA104/105/107 minidiskette write protected and unprotected.

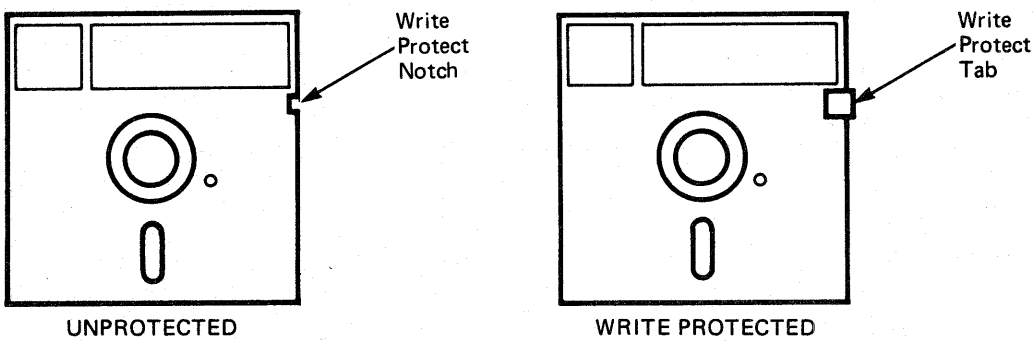
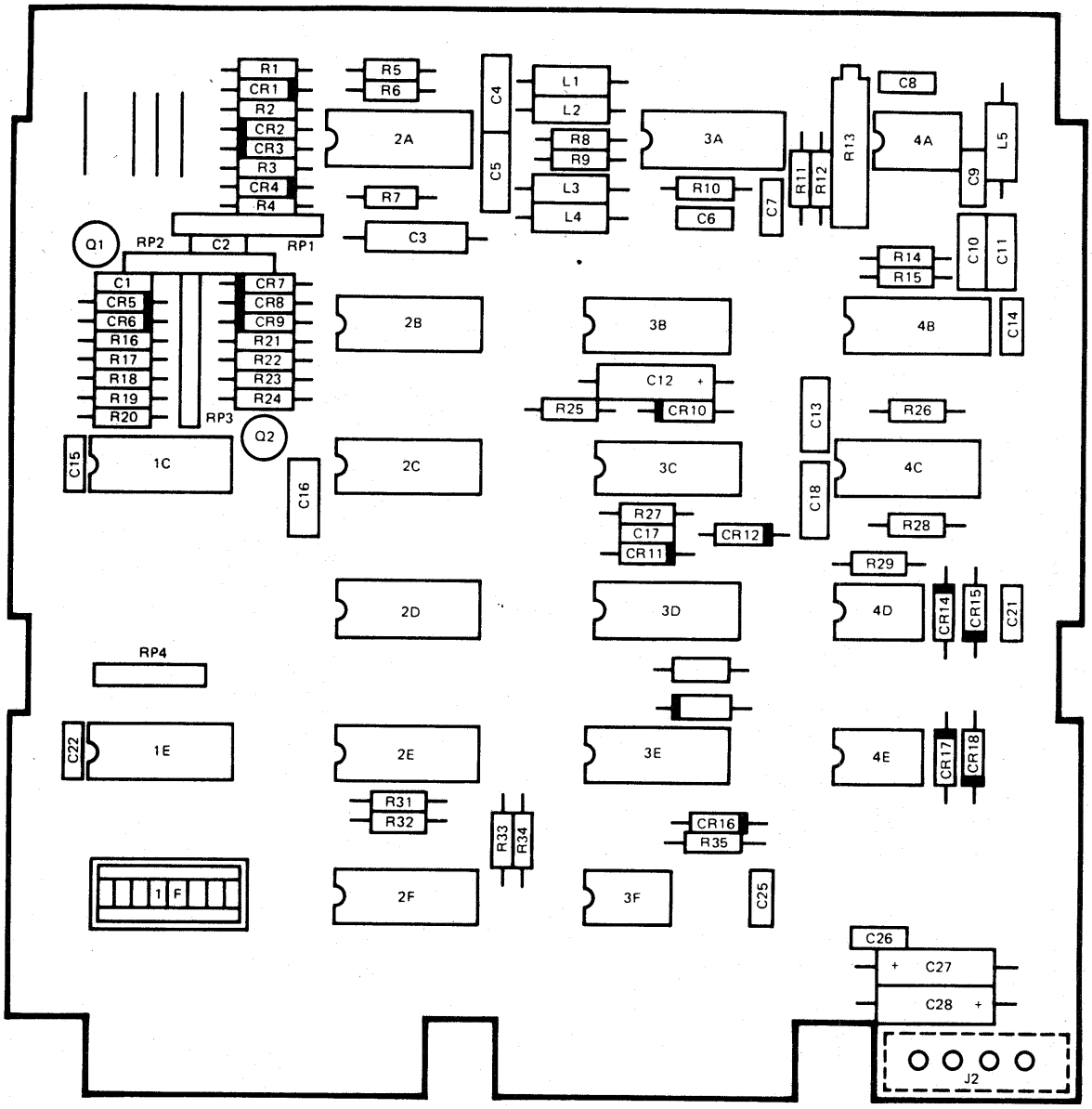
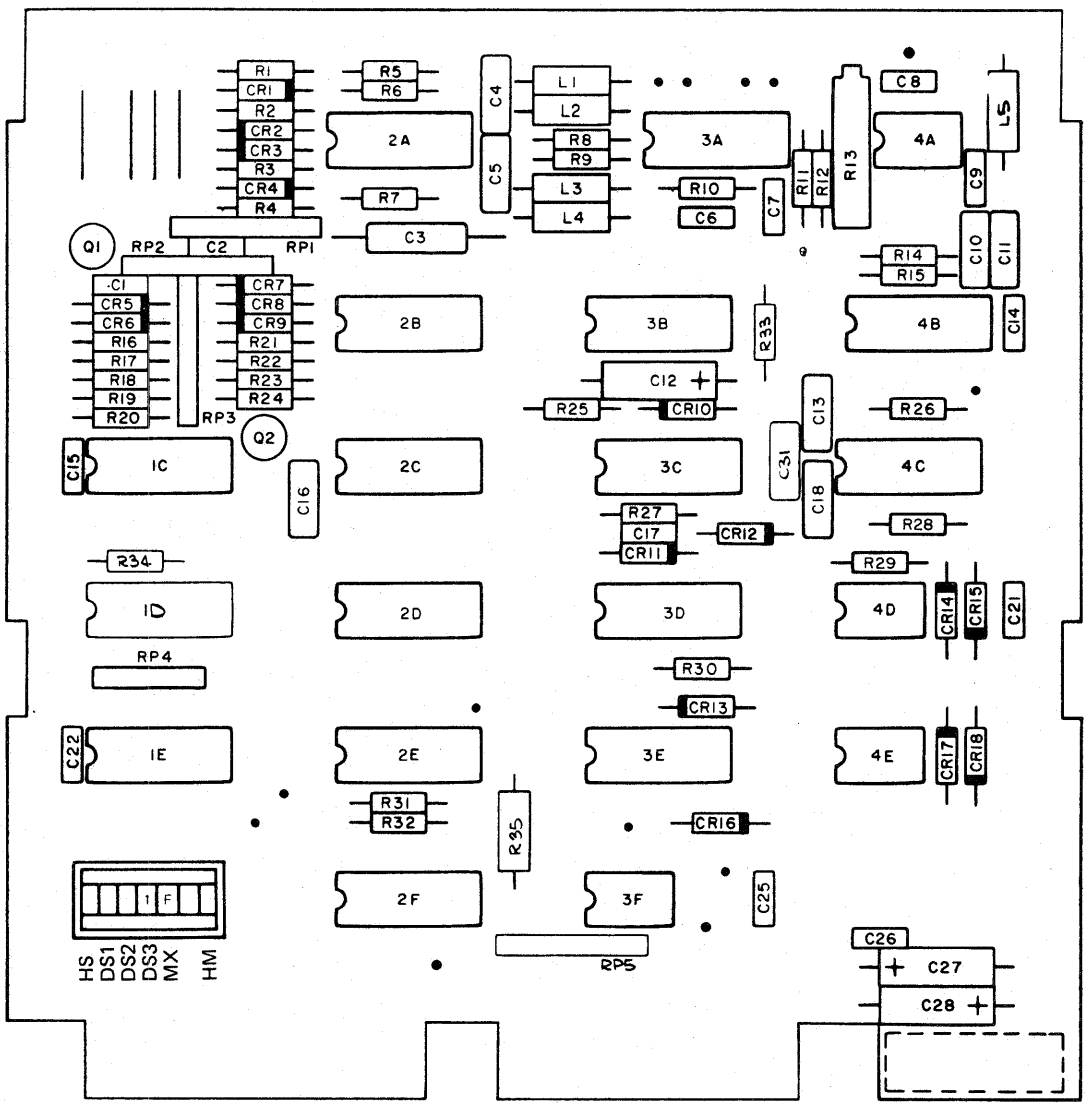


FIGURE 38. SA104/105/107 WRITE PROTECT



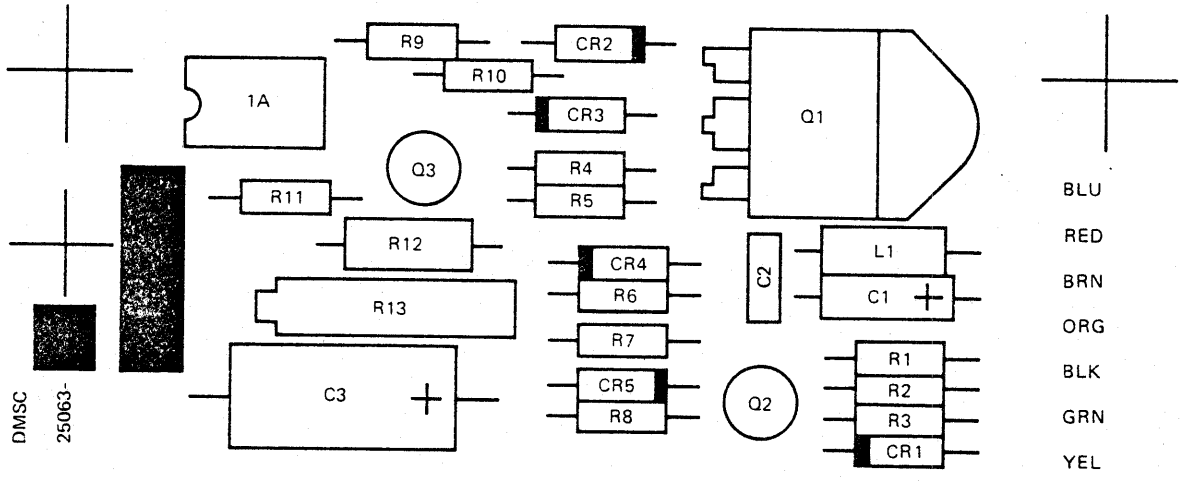
DRIVE PCB
COMPONENT LOCATIONS
BELOW E.C. 649



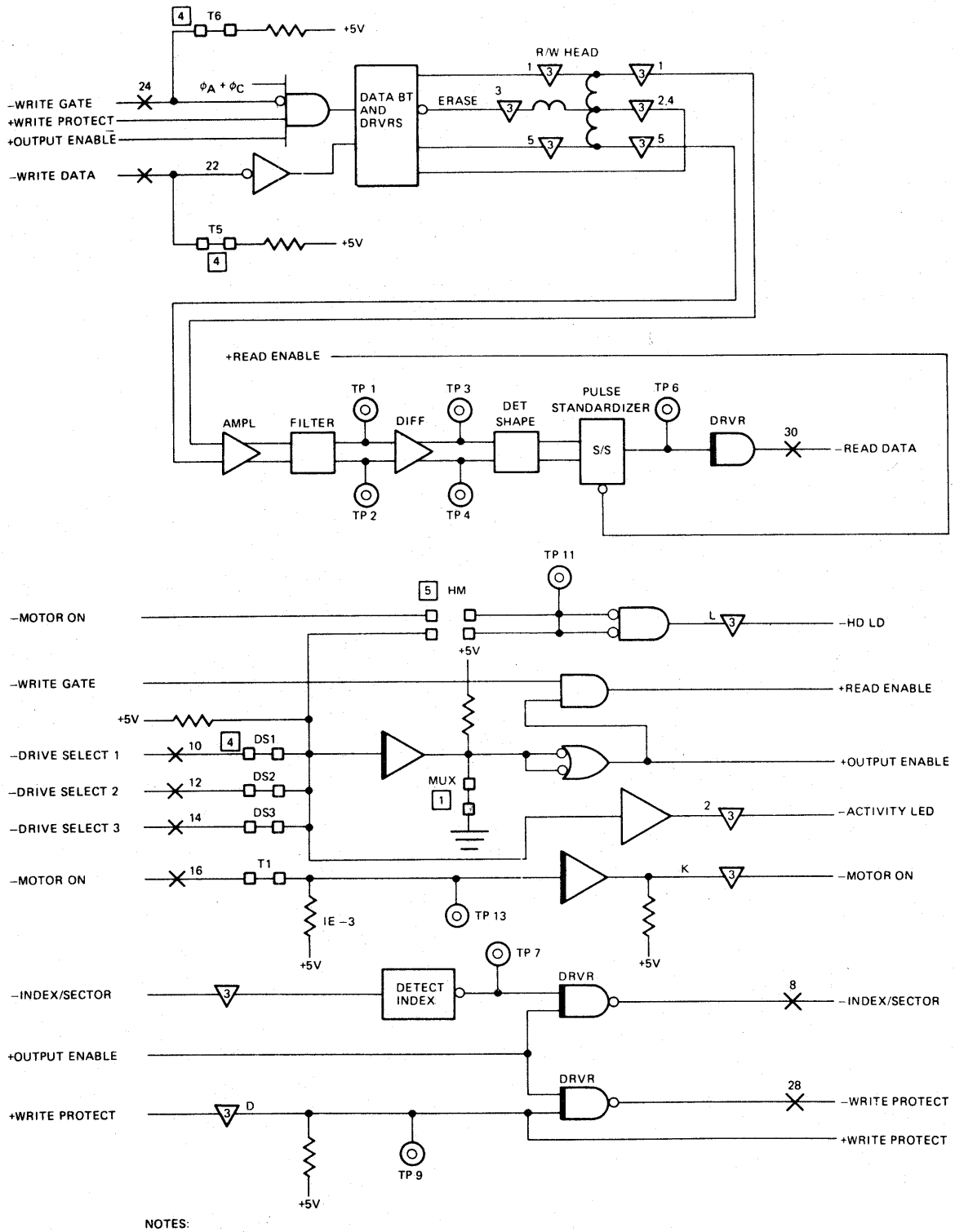
● TEST POINTS

DRIVE PCB
COMPONENT LOCATIONS

E.C. 649 AND ABOVE



MOTOR CONTROL PCB
COMPONENT LOCATIONS

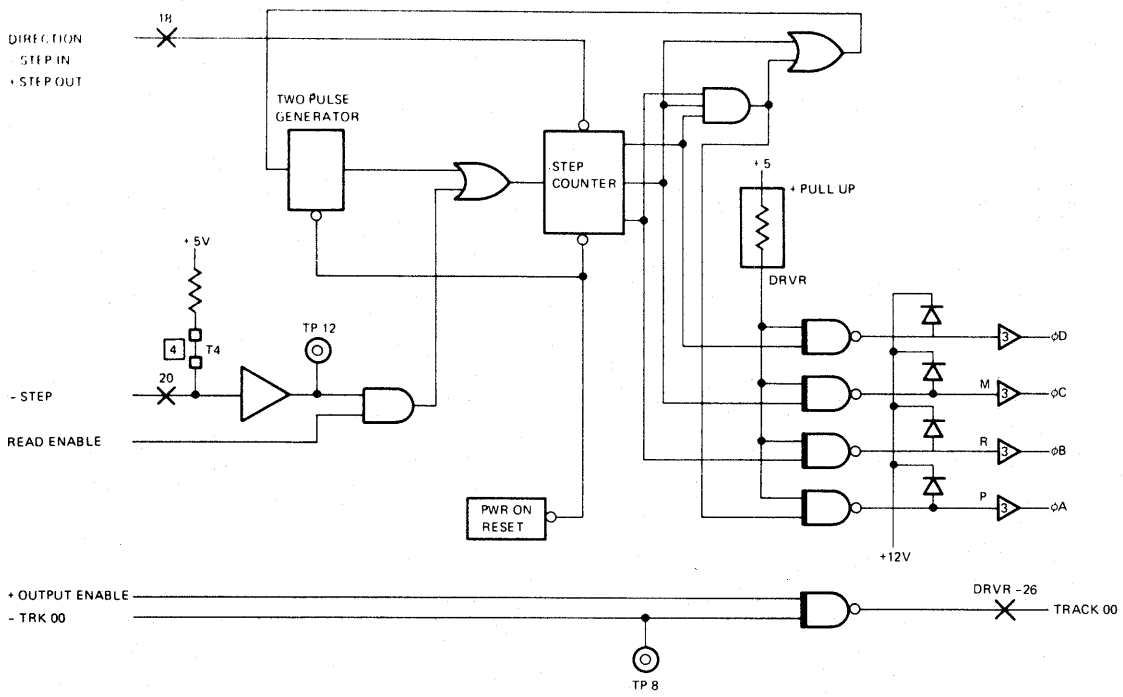


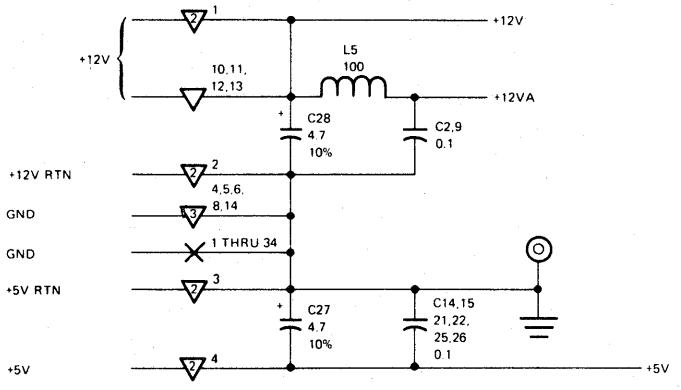
NOTES:

1. CUT TRACE OPTION FOR MULTIPLEX OPERATION
2. CONNECTOR SYMBOL REFERENCE — X = J1, 2 = J2, 3 = J3, 4 = J4
3. ALL ODD NUMBERED PINS ON J1 CONNECTOR ARE GROUND
4. PROGRAM SHUNT
5. WITH HM SHORTED HEAD LOADS WITH -MOTOR ON
   WITH HS SHORTED HEAD LOADS WITH -DRIVE SELECT

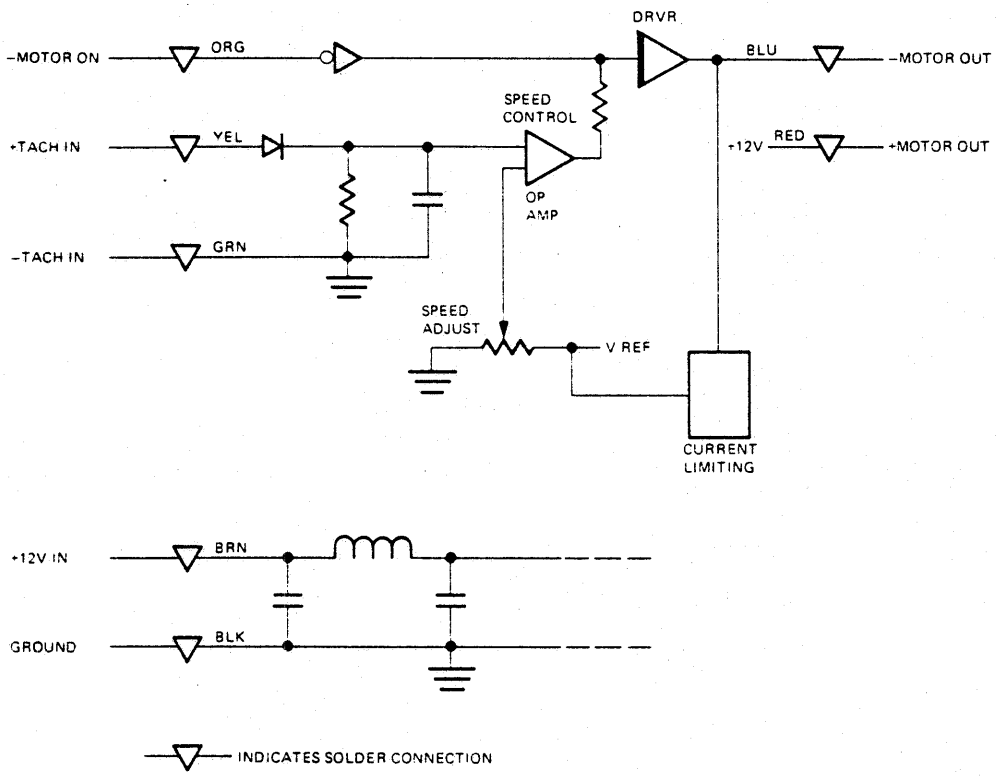
DRIVE PCB LOGIC DIAGRAM PCBP/N 25060
READ/WRITE, INDEX,
WRITE PROTECT, DRIVE SELECTION

1 OF 2

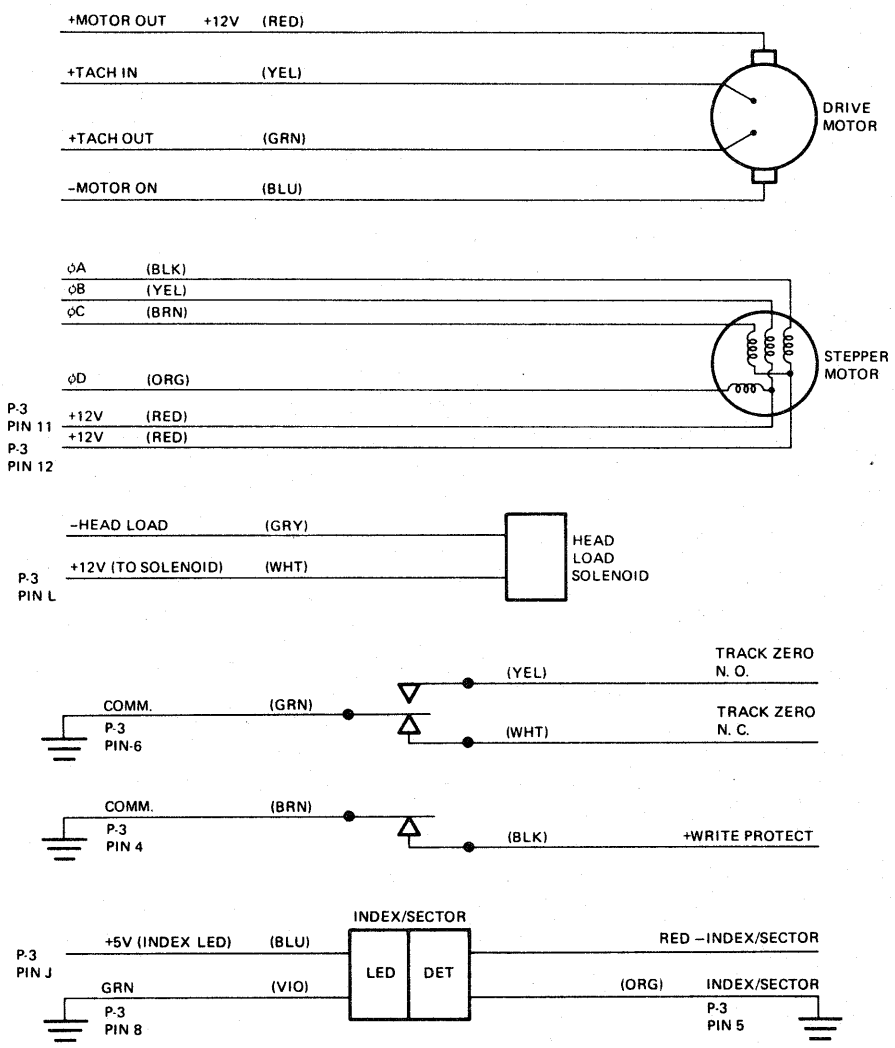




DRIVE PCB
STEPPER CONTROLS, TRACK ZERO,
POWER



MOTOR SPEED CONTROL PCB LOGIC DIAGRAM
AMPLITUDE MODULATION PCB P/N 25062



SWITCH AND MOTOR CONNECTIONS

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DESCRIPTION

General

The Illustrated Parts Catalog is arranged so that the figures precede the parts listings and will be on the opposite page.

The drive assembly is contained on a single page. Sub assemblies will be separated by a solid line and are broken down on this page.

Indented Level

The parts list is indented to show the levels of assembly within a figure. The major assembly will always be level 1, all parts or assemblies that attach to that assembly will be level 2 and assemblies within level 2 will have their attaching parts level 3 and so on.

Parts Replacement

Some parts and assemblies are not field replaceable. These will be noted by an asterisk* and a footnote. These part numbers are included so they can be ordered for factory and/or repair centers.

Quantity Per Assembly

The quantity listed is the quantity used on the assembly.

Numerical Index

The numerical index lists all parts in part number sequence and is cross referenced to the figure and reference number.

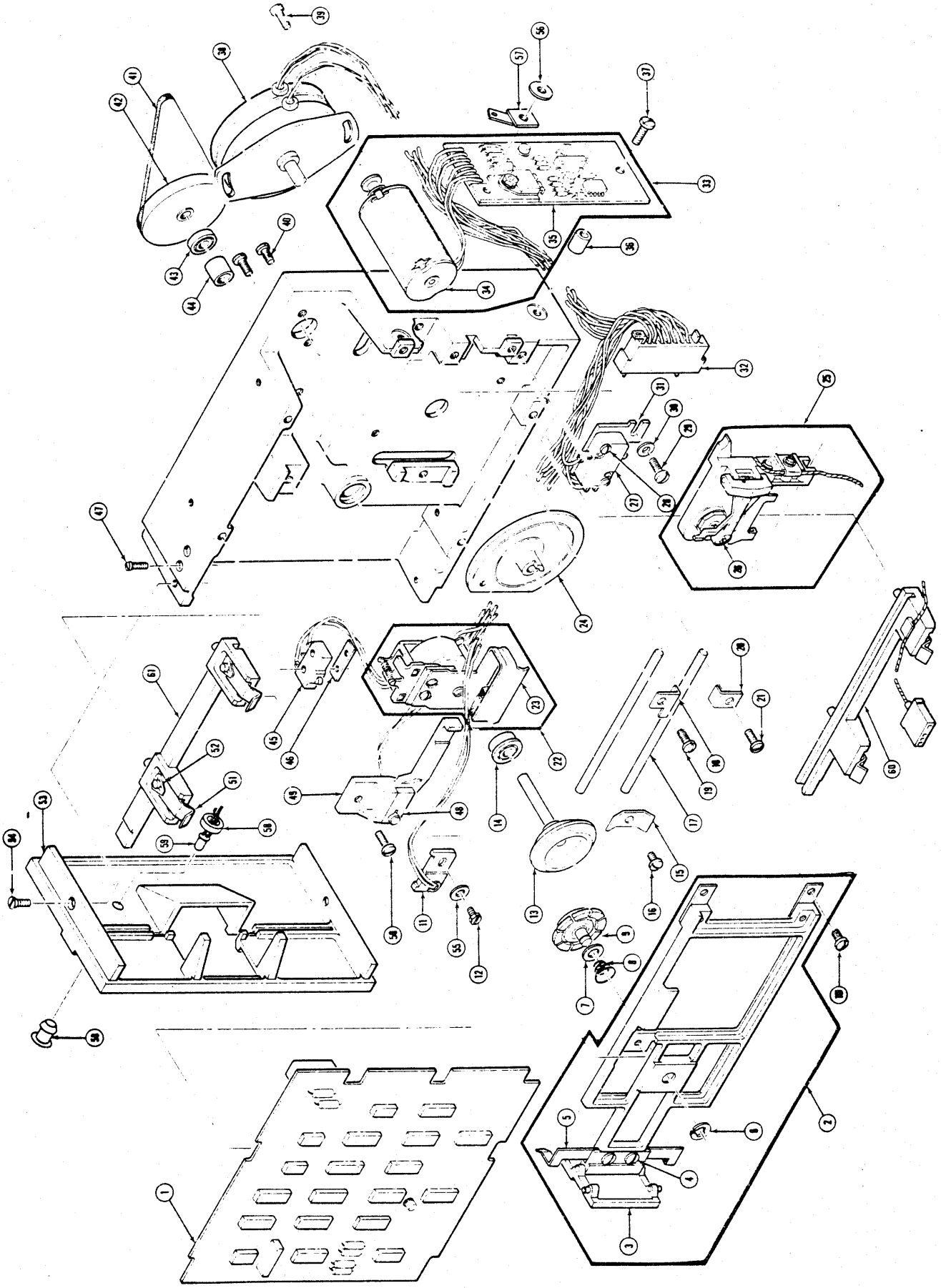


FIGURE & REF. NUMBER	PART NUMBER	DESCRIPTION 1 2 3 4	QTY PER ASM
1			
		DRIVE ASSEMBLY	
- 1	25060	. PCB, DRIVE	1
- 2	54070	. HUB FRAME ASSEMBLY	1
- 3	54073	. . DOOR HINGE	1
- 4	10186	. . SCREW 6-32 X .188 BH	2
- 5	54057	. . STOPDISK	1
- 6	11305	. . E-RING	1
- 7	54131	. . COLLAR HUB	1
- 8	54132	. . SPRING, CLAMP	1
- 9	54066	. . HUB, COLLETT	1
-10	10186	. SCREW 6-32X.188 BH	2
-11	54136	. DETECTOR INDEX	1
-12	10187	. SCREW 6-32X.188 BH	1
-13	* 54032	. SPINDLE	1
-14	* 10805	. BEARING, FLANGED	1
-15	54078	. KEEPER, GUIDE ROD	1
-16	10186	. SCREW 6-32X.188 BH	1
-17	54006	. GUIDE ROD	2
-18	54099	. STOP, CARRIAGE	1
-19	10186	. SCREW 6-32X.188 BH	1
-20	54078	. KEEPER GUIDE ROD	1
-21	10186	. SCREW 6-32X.188 BH	1
-22	54064	. SOLENOID ASSMY. HEAD LOAD	1
-23	54135	. . BAIL, LOAD	1
-24	54003	. CAM, ACTUATOR	1
-25	54055	. HEAD & CARRIAGE ASSMY.	1
-26	54145	. . LOAD BUTTON	1
-27	17211	. TK 00 SWITCH	1
-28	10176	. SCREW 4-40X.50 BH	2
-29	10187	. SCREW 6-32X.250 BH	1
-30	10013	. WASHER	1
-31	54038	. MOUNT TK 00 SWITCH	1
-32	15655	. CONNECTOR P-3	1
-33	54067	. MOTOR & CONTROL ASSEMBLY	1
-34	54047	. . MOTOR DRIVE	1
-35	25063	. . PCB MOTOR CONTROL	1
-36	54069	. STANDOFF, MOTOR PCB	2
-37	10191	. SCREW 6-32X.50 BH	2
-38	* 54068	. MOTOR, STEPPER	1
-39	10187	. SCREW 6-32X.250 BH	2
-40	10177	. SCREW 4-40X.625 BH	2
-41	54048	. BELT, DRIVE	1
-42	* 54138	. PULLEY, SPINDLE	1
-43	* 10804	. BEARING	1
-44	* 54097	. SPACER, LONG	1
-45	17212	. SWITCH WRITE PROTECT	1
-46	54062	. NUT PLATE	1
-47	10166	. SCREW 2-56X.50 BH	1
-48	54137	. LED, INDEX	1
-49	54125	. PLATEN	1
-50	10189	. SCREW 6-32X.250 BH	1
-51	54036	. CLAMP, PCB	4
-52	11311	. RETAINER, CLAMP	4
-53	54077	. FACEPLATE	1
-54	11900	. 6-32X.250 F.H.	2
-55	10013	. WASHER	1
-56	12501	. WASHER	1
-57	15663	. FASTON	1
-58	11312	. ACTIVITY LIGHT HOLDER	1
-59	15915	. LED ACTIVITY LIGHT	1
-60	* 54089	. GUIDE DISKETTE R.H.	1
-61	* 54090	. GUIDE DISKETTE L. H.	1
		* NOT FIELD REPLACEABLE	

PART NUMBER	REF.
10013	55
10166	47
10176	28
10177	40
10186	4
	10
	12
	16
	19
	21
10187	12
	29
	39
10189	50
10191	37
10804	43
10805	14
11305	6
11311	52
11312	58
11900	54
12501	56
15655	32
15663	57
17211	27
17212	45
25060	1
25063	35
54003	24
54006	17
54032	13
54036	51
54038	31
54047	34
54048	41
54055	25
54057	5
54062	46
54064	22
54065	36
54066	9
54067	33
54068	38
54070	2
54073	3
54077	53
54078	15
	20

PART NUMBER	REF.
54089	60
54090	61
54097	44
54099	18
54125	49
54131	7
54132	8
54135	23
54136	11
54137	48
54138	42
54145	26

TEI INC.

5075 S. Loop East
Houston, Texas 77033

713-738-2300
TWX: 1-910-881-3639

SECTION X
STANDARD-FLOPPY DISK DRIVE
(800 SERIES)
TEI INC.

P/N 13686-10

SECTION X

MCS-DFD 80/DFD 85

MCS-RFD 80/RFD 85

		PAGE
I.	MCS-DFD/RFD	
	A. OUTLINE DRAWING	10-2
	B. INTRODUCTION	10-3
	C. POWER SUPPLY PC BOARD	10-4
	D. PARTS LIST	10-4
	E. SCHEMATIC DIAGRAM	10-5
II.	SA 800 DRIVE	
	A. GENERAL DESCRIPTION	10-7
	B. FUNCTIONAL CHARACTERISTICS	10-11
	C. FUNCTIONAL OPERATIONS	10-13
	D. ELECTRICAL INTERFACE	10-19
	E. CUSTOMER INSTALLABLE OPTIONS	10-25
	F. OPERATING PROCEDURES	
	G. LOGIC DIAGRAMS	10-31
III.	SA 850 DRIVE	N/A

INTRODUCTION:

THE TEI, INC. MCS - DFD (DUAL FLOPPY DISK) IS A PAIR OF SHUGART SA-800 DRIVES WITH SINGLE HEADS, OR SA-850 DRIVES WITH DUAL HEADS. THESE DRIVES MAY BE EITHER SINGLE OR DUAL DENSITY. THE DRIVES ARE ALL SOFT SECTORED, IBM COMPATIBLE, AND WILL HOLD THE FOLLOWING VOLUMES OF DATA:

TEI, INC. MODEL			MEMORY CAPACITY
MCS-DFD 80	S	(SINGLE HEAD, SINGLE DENSITY)	512 BYTES
MCS-DFD 80	D	(SINGLE HEAD, DUAL DENSITY)	1 MEGABYTES
MCS-DFD 85	S	(DUAL HEADS, SINGLE DENSITY)	1 MEGABYTES
MCS-DFD 85	D	(DUAL HEADS, DUAL DENSITY)	2 MEGABYTES

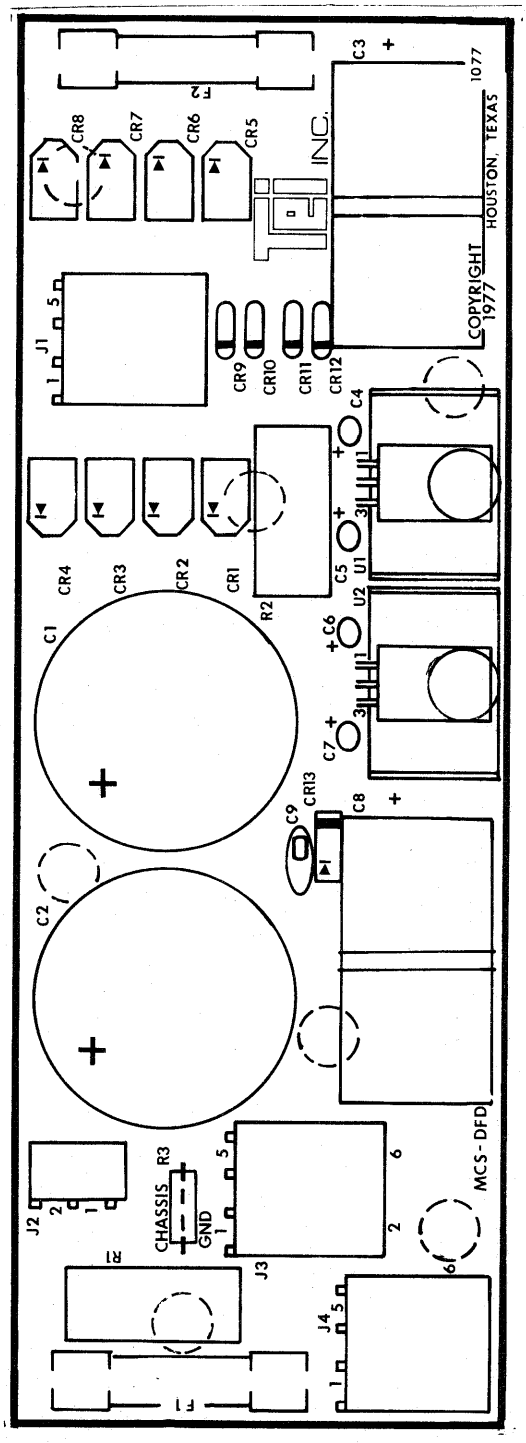
ALL THE TEI, INC. FLOPPY DISK DRIVES ARE BUILT WITH RUGGED INDUSTRIAL QUALITY CHASSIS AND ARE POWERED BY A HIGH QUALITY CVT (CONSTANT VOLTAGE TRANSFORMER) TO PROTECT YOUR SYSTEM FROM POWER FLUCTUATIONS.

NOTE: THE MCS-RFD 80/85 IS THE SAME AS THE MCS-DFD 80/85 EXCEPT THAT IT IS CONTAINED IN A RUGGEDIZED 7" x 19" RACK PANEL WITH CHASSIS SLIDES AND BRACKETS FOR MOUNTING IN PANEL RACKS UP TO 28" DEEP.

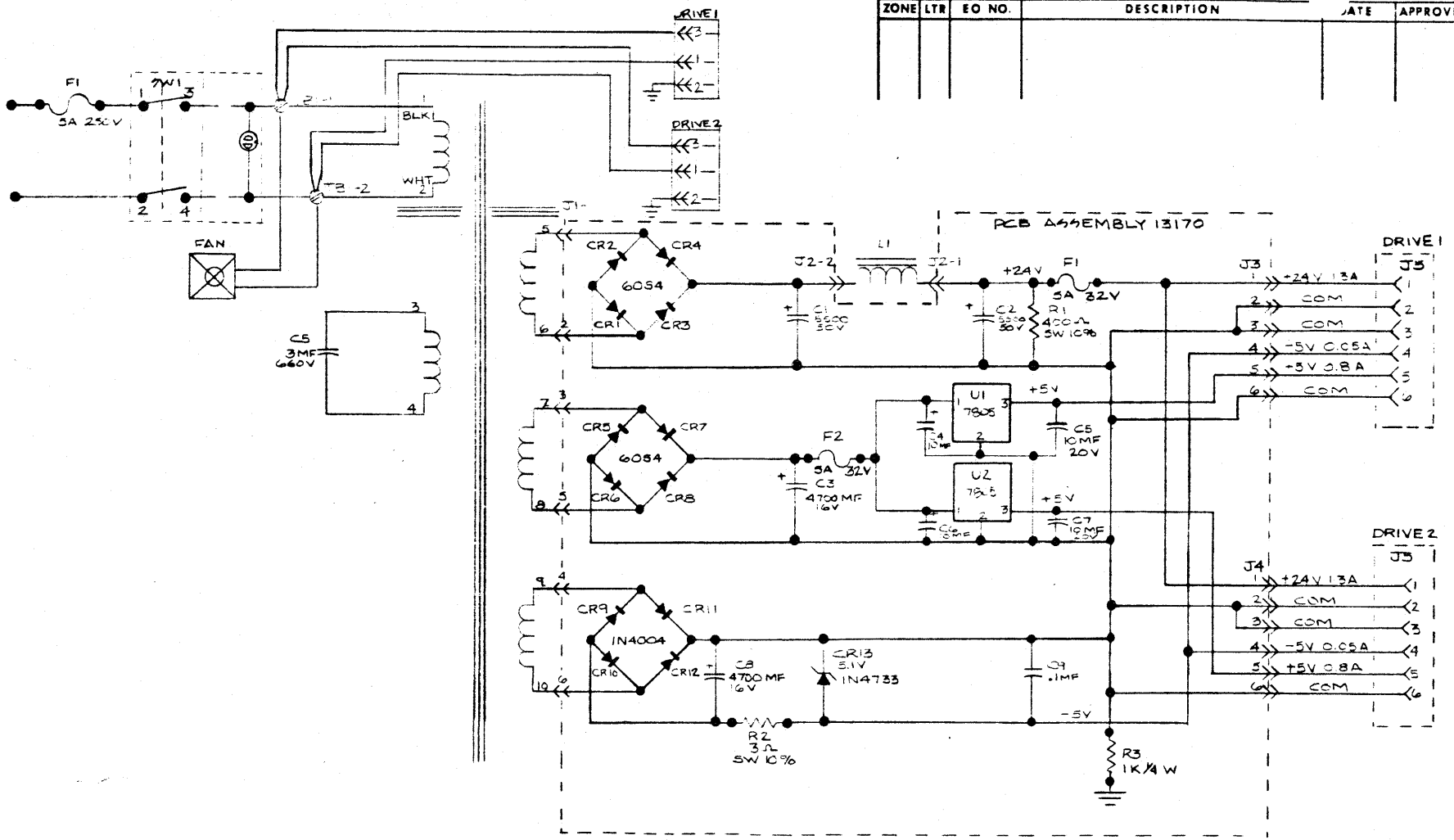
PARTS LIST

MCS-DFD 80

REF DES	DESCRIPTION	TEI P/N
	CHASSIS MOUNTED PARTS	
BL1	FAN	2610-010
C1	CAP 3MF, 660VAC	1543-006
D1,D2	Disk Drives, 800	13331
F1	FUSE SA 250V	5173-022
J1,J3, J4	Socket Housing, 6CKT	2122-010
J2	Socket Housing, 2CKT	2122-021
Drive Conn	Socket Housing, 4CKT	2122-009
Drive Conn	Socket Housing, 3CKT	2122-026
L1	Choke	11010
PCD1	Power Supply	13170
SW1	Power Switch	5113-001
T1	Transformer	13239
TB1	Barrier Strip, 4 POS	2171-025
	Boot, Rubber AC Cap	1592-003
	Fan Filter	13146
	Feet, Rubber	1419-001
	Power Cord	6080-008
	Ribbon Cable	13425
	PCB1 POWER SUPPLY	
C1,C2	Cap 5500MF, 50V	1521-089
C3,C8	Cap 4700MF, 16V	1527-074
C4 Thru C7	Cap 10MF, 20V	1580-001
CR1 Thru CR8	Diode 3 AMP	4825-043
CR9 Thru CR12	Diode IN4004	4820-005
CR13	Diode IN5338B	4840-041
F1	Fuse 5A 32V	5173-021
F2	Fuse 4A 250V	5173-020
J1,J3, J4	Pin Header, 6CKT	2122-004
J2	Pin Header, 2CKT	2122-020
PCB1	PCB FAB	13171
R1	Resistor 400 Ω 5W 10%	4755-299
R2	Resistor 3 Ω 5W 10%	4755-095
CHASSIS GND	Resistor 1 K 1/4 W 2%	4741-337
U1,U2	Regulator 7805	3120-003
	Heat Sink	4890-002



REVISIONS					
ZONE	LTR	EO NO.	DESCRIPTION	DATE	APPROVED



QTY	PART NUMBER	DESCRIPTION	MANUFACTURER	CODE IDENT	REF DES	ITEM
		PARTS LIST				

NEXT ASSY	USED ON
APPLICATION	

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.X ± .06
.XX ± .02
.XXX ± .010
ANGULAR ± .5 DEG

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

MATERIAL

CONTRACT NO.

SIGNATURES	DATE
DR	6-7-77
DES	
CHK	
ENGR	
APP	
APP	

TEXAS ELECTRONIC INSTRUMENTS, INC
HOUSTON, TEXAS

DUAL FLOPPY DISC
SCHEMATIC

SIZE	CODE IDENT NO.	DWG NO.	REV
C	33179	13278	

SCALE | REL EO NO. | SHEET OF

10-5

NOTES:

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1.0 INTRODUCTION

1.1 General Description

The SA800/801 are enhanced versions of the successful SA900/901 Diskette Storage Drive. The SA800/801 provides the customer with a mature and reliable product, manufactured to the same high standard of excellence as the 900/901, but with additional features.

The SA800 Diskette Storage Drive can read and write diskettes for interchange with other SA800's, the SA900, IBM 3741, 3742 or 3540 and with the new IBM System 32.

The SA801 provides the same features as the SA800 with additional flexibility for those requirements which preclude IBM compatibility.

The SA800/801 Diskette Storage Drives have as standard features: a patented diskette clamping/registration design which eliminates the possibility of damage to the diskette due to misregistration and guarantees over 30,000 interchanges with each diskette; single and double density capability on the same drive for the same price; a proprietary ceramic R/W head designed and manufactured by Shugart Associates to provide media life exceeding 3.5 million passes/track and head life exceeding 15,000 hours; an activity light which indicates drive in use; and ribbon cable or twisted pair connector for ease of packaging. All of these features and more are available with the SA800/801.

SA800/801 Diskette Storage Drives provide the system designer solutions to his applications requirements with greater performance and reliability than cassette or cartridge drives, and lower cost with increased function over card I/O and reel-to-reel tape drives.

Applications for the SA800/801 Diskette Storage Drive are key entry systems, point of sale recording systems, batch terminal data storage, microprogram load and error logging, minicomputer program and auxiliary data storage, word processing systems and data storage for small business systems.

The SA100 Diskette, IBM Diskette or equivalent, can be read and written interchangeably between any SA800 and IBM 3741/42, 3747 and 3540. The SA101 Diskette can be read or written interchangeably on any SA801.

1.2 Specification Summary

1.2.1 Performance Specifications

Capacity	Single Density	Double Density
Unformatted		
Per Disk	3.2 megabits	6.4 megabits
Per Track	41.7 kilobits	83.4 kilobits
IBM Format		
Per Disk	2.0 megabits	n/a
Per Track	26.6 kilobits	n/a
Transfer Rate	250 kilobits/sec	500 kilobits/sec
Latency (average)	83 ms	83 ms
Access Time		
Track to Track	8 ms	8 ms
Average	260 ms	260 ms
Settling Time	8 ms	8 ms
Head Load Time	35 ms	35 ms

1.2.2 Functional Specifications

	Single Density	Double Density
Rotational Speed	360 rpm	360 rpm
Recording Density		
(inside track)	3200 bpi	6400 bpi
Flux Density	6400 fci	6400 fci
Track Density	48 tpi	48 tpi
Tracks	77	77
Physical Sectors		
SA800	0	0
SA801	32/16/8	32/16/8
Index	1	1
Encoding Method	FM	M^2FM
Media Requirements		
SA800	SA100/IBM Diskette	SA102/IBM Diskette
SA801	SA101	SA103

1.2.3 Physical Specifications

Environmental Limits
- Ambient Temperature = 40°F to 115°F (4.4°C to 46.1°C)
- Relative Humidity = 20% to 80%
- Maximum Wet Bulb = 78°F (25°C)

AC Power Requirements

50/60 Hz ± 0.5 Hz
- 100/115 VAC Installations = 85 to 127 V @ .4A typical
- 200/230 VAC Installations = 170 to 253 V @ .2A typical

DC Voltage Requirements

+24 VDC ± 5% 1.3A typical
+ 5 VDC ± 5% 0.8A typical
- 5 VDC ± 5% .05A typical (option -7 to -16 VDC)

Mechanical Dimensions (Reference Figures 18 and 18A)
- Width = 4 5/8 in. (11.75 cm)
- Height = 9 1/2 in. (24.13 cm)
- Depth = 14 1/4 in. (36.20 cm)
- Weight = 13.0 lbs. (5.91 kg)

Heat Dissipation = 271 BTU/hr. typical

1.2.4 Reliability Specifications

MTBF:	5000 POH under heavy usage 8000 POH under typical usage.
PM:	Every 5000 POH under heavy usage. Every 15,000 POH under typical usage.
MTTR:	30 minutes.
Component Life:	15,000 POH.
Error Rates:	
Soft Read Errors:	1 per 10^9 bits read.
Hard Read Errors:	1 per 10^{12} bits read.
Seek Errors:	1 per 10^6 seeks.
Media Life:	
Passes per Track	3.5×10^6
Insertions:	30,000+

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2.0 FUNCTIONAL CHARACTERISTICS

2.1 General Operation

The SA800/801 Diskette Storage Drive consists of read/write and control electronics, drive mechanism, read/write head, track positioning mechanism, and the removable diskette. These components perform the following functions:

Interpret and generate control signals.
Move read/write head to the selected track.
Read and write data.

The relationship and interface signals for the internal functions of the SA800/801 are shown in Figure 2.

The Head Positioning Actuator positions the read/write head to the desired track on the diskette. The Head Load Actuator loads the diskette against the read/write head and data may then be recorded or read from the diskette.

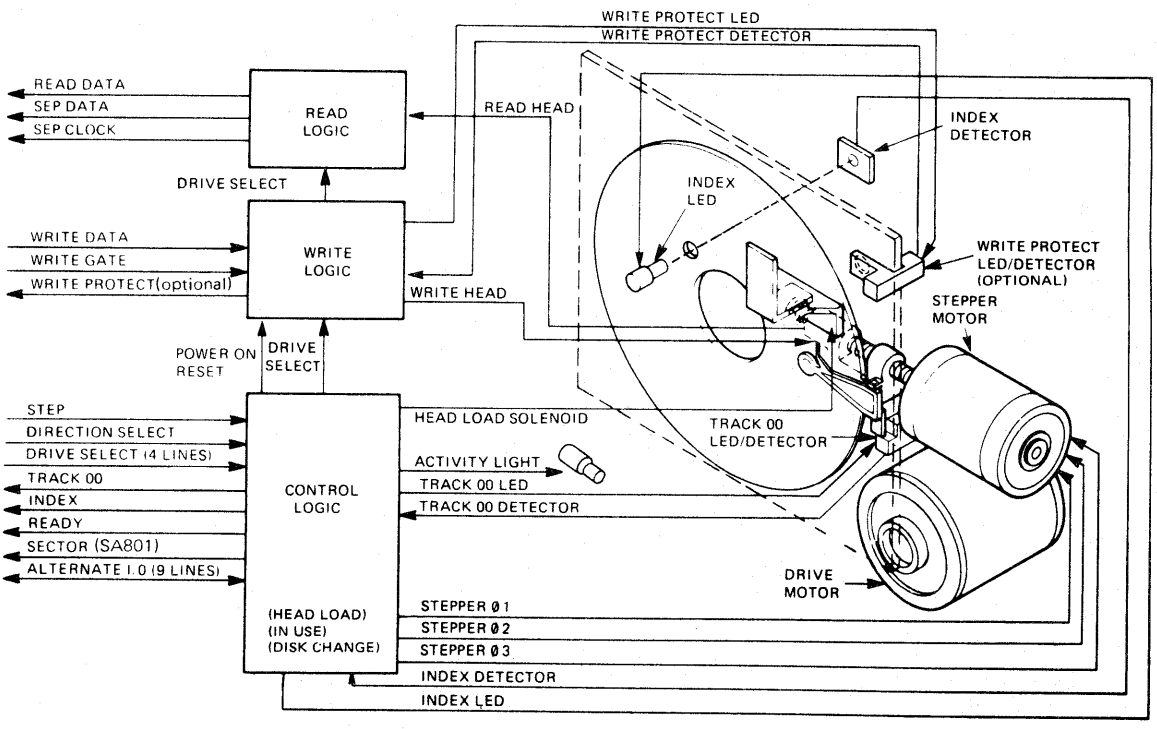


Figure 2. SA800/801 Functional Diagram

2.2 Read/Write and Control Electronics

The electronics are packaged on one PCB. The PCB contains:

1. Index Detector Circuits (Sector/Index for 801)
2. Head Position Actuator Driver
3. Head Load Actuator Driver
4. Read/Write Amplifier and Transition Detector
5. Data/Clock Separation Circuits
6. Write Protect
7. Drive Ready Detector Circuit
8. Drive Select Circuits

2.3 Drive Mechanism

The Diskette drive motor rotates the spindle at 360 rpm through a belt-drive system. 50 or 60 Hz power is accommodated by changing the drive pulley and belt. A registration hub, centered on the face of the spindle, positions the Diskette. A clamp that moves in conjunction with the cartridge guide fixes the Diskette to the registration hub.

2.4 Positioning Mechanism

An electrical stepping motor (Head Position Actuator) and lead screw positions the read/write head. The stepping motor rotates the lead screw clockwise or counterclockwise in 15° increments. A 15° rotation of the lead screw moves the read/write head one track position. The using system increments the stepping motor to the desired track.

2.5 Read/Write Head

The SA800/801 head is a single element ceramic read/write head with straddle erase elements to provide erased areas between data tracks. Thus normal interchange tolerances between media and drives will not degrade the signal to noise ratio and insures Diskette interchangeability.

The read/write head is mounted on a carriage which is located on the Head Position Actuator lead screw. The Diskette is held in a plane perpendicular to the read/write head by a platen located on the base casting. This precise registration assures perfect compliance with the read/write head. The Diskette is loaded against the head with a load pad actuated by the head load solenoid.

The read/write head is in direct contact with the Diskette. The head surface has been designed to obtain maximum signal transfer to and from the magnetic surface of the Diskette with minimum head/Diskette wear.

2.6 Recording Format

The format of the data recorded on the disk is totally a function of the host system, and can be designed around the users application to best take advantage of the total available bits that can be written on any one track.

For a detailed discussion of various recording formats, the systems designer should read one of the following:

1. IBM Compatibility Manual
2. Shugart Associates Double Density Design Guide
3. SA801/901 Track Formats

2.7 Optional Features

1. -12 to -15 Volt DC to replace -5 Volt DC required.
2. Dust Cover. Not available on "R" series.
3. Write Protect for SA800. Standard on SA801.
4. Door Lock. Will lock the door when drive is selected or through alternate I/O pin.
5. Horizontal mounting with door opening up.
6. SA800/801 "R" Series. Allows two drives to be horizontally installed in a standard 19" Retma rack. Reference figure 18A.

3.0 FUNCTIONAL OPERATIONS

3.1 Power Sequencing

Applying AC and DC power to the SA800/801 can be done in any sequence, however, once AC power has been applied, a 2 second delay must be introduced before any Read or Write operation is attempted. This delay is for stabilization of the Diskette rotational speed. Also, after application of DC power, a 90 millisecond delay must be introduced before a Read, Write, or Seek operation or before the control output signals are valid. After powering on, initial position of the R/W head with respect to data tracks is indeterminant. In order to assure proper positioning of the R/W head prior to any read/write operation after powering on, a Step Out operation should be performed until the Track 00 indicator becomes active.

3.2 Drive Selection

Drive selection occurs when a drive's Drive Select line is activated. Only the drive with this line active will respond to input lines or gate output lines. Under normal operation, the Drive Select line will load the R/W head, apply power to the stepper motor, enable the input lines, activate the output lines and light the Activity LED on the front of the drive. Optional modes of operation are traces. Reference section 7 for these user installable features.

3.3 Track Accessing

Seeking the R/W head from one track to another is accomplished by:

a. Activating Drive Select line.

b. Selecting desired direction utilizing Direction Select line.

c. Write Gate being inactive.

d. Pulsing the Step line.

Multiple track accessing is accomplished by repeated pulsing of the Step line until the desired track has been reached. Each pulse on the Step line will cause the R/W head to move one track either in or out depending on the Direction Select line. Head movement is initiated on the trailing edge of the Step Pulse.

3.3.1 Step Out

With the Direction Select line at a plus logic level (2.5V to 5.25V) a pulse on the Step line will cause the R/W head to move one track away from the center of the disk. The pulse(s) applied to the Step line and the Direction Select line must have the timing characteristics shown in Figure 3.

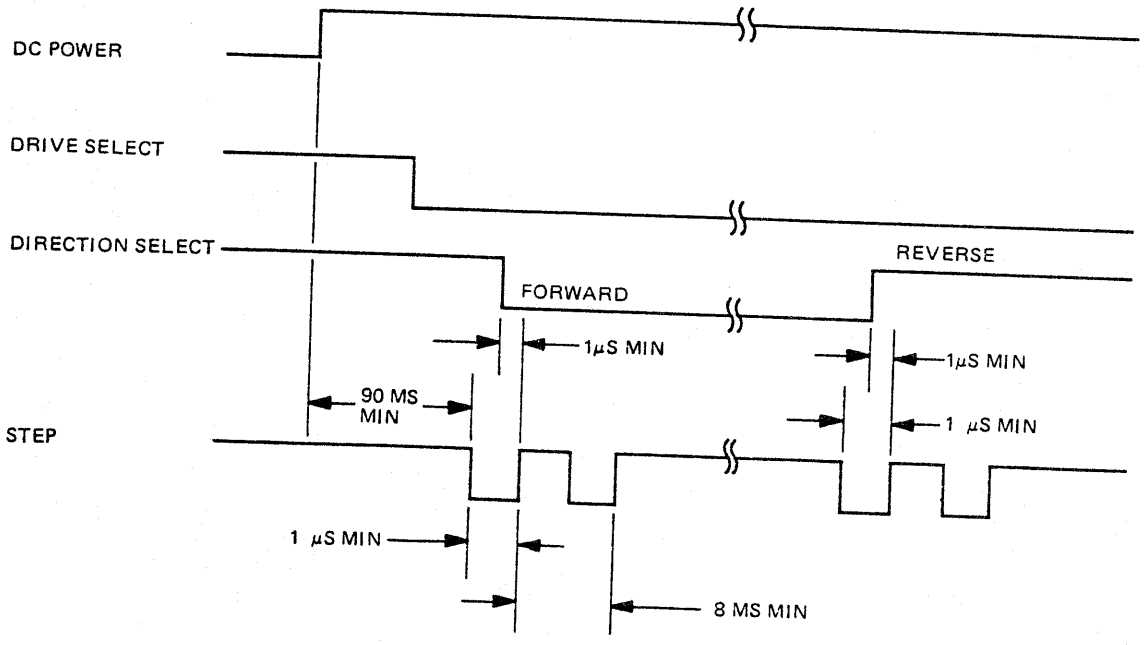
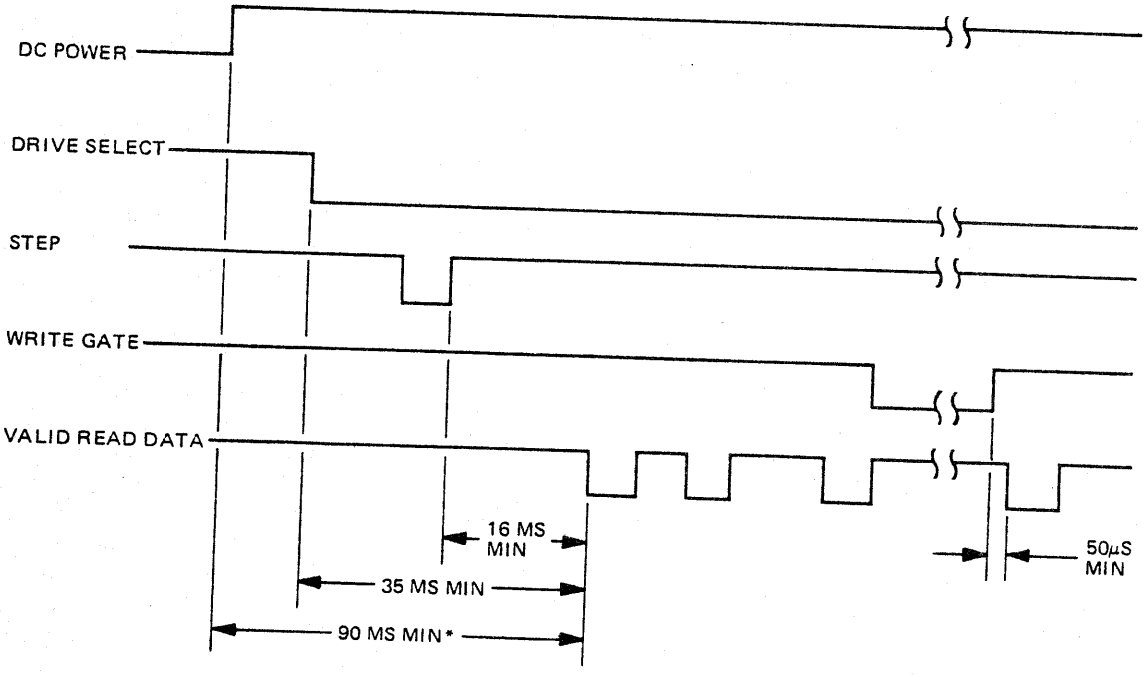


Figure 3. Track Access Timing



* 2 SECONDS IF AC AND DC POWER ARE APPLIED AT SAME TIME

Figure 4. Read Initiate Timing

3.3.2 Step In

With the Direction Select line at a minus logic level (0V to .4V), a pulse on the Step line will cause the R/W head to move one track closer to the center of the disk. The pulse(s) applied to the Step line must have the timing characteristics shown in Figure 3.

3.4 Read Operation

Reading data from the SA800/801 Diskette Storage drive is accomplished by:

a. Activating Drive Select line.

b. Write Gate being inactive.

The timing relationships required to initiate a read sequence are shown in Figure 4. These timing specifications are required in order to guarantee that the R/W head position has stabilized prior to reading.

The timing of the read signals, Read Data, Separated Data, and Separated Clock are shown in Figure 5.

3.5 Write Operation

Writing data to the SA800/801 is accomplished by:

a. Activating the Drive Select line.

b. Activating the Write Gate line.

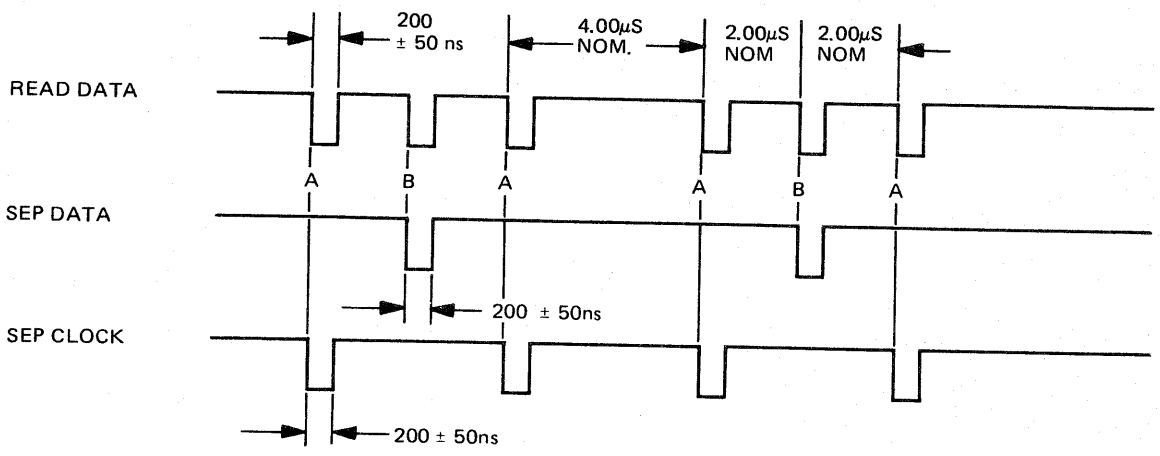
c. Pulsing the Write Data line with the data to be written.

The timing relationships required to initiate a write data sequence are shown in Figure 6. These timing specifications are required in order to guarantee that the R/W head position has stabilized prior to writing.

The timing specifications for the Write Data pulses are shown in Figure 7.

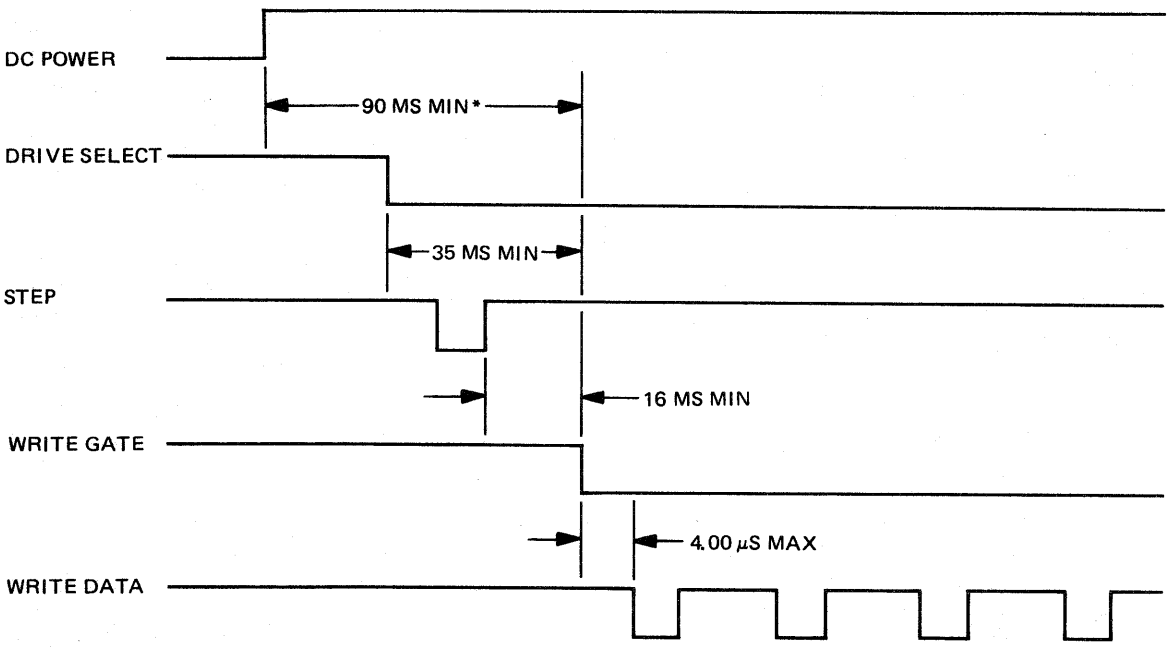
3.6 Sequence of Events

The timing diagram shown in Figure 8 shows the necessary sequence of events with associated timing restrictions for proper operation.



A = LEADING EDGE OF BIT MAYBE ± 400 ns FROM ITS NOMINAL POSITION.
B = LEADING EDGE OF BIT MAYBE ± 200 ns FROM ITS NOMINAL POSITION.

Figure 5. Read Signal Timing



* 2 SECONDS IF AC AND DC POWER ARE APPLIED AT SAME TIME.

Figure 6. Write Initiate Timing

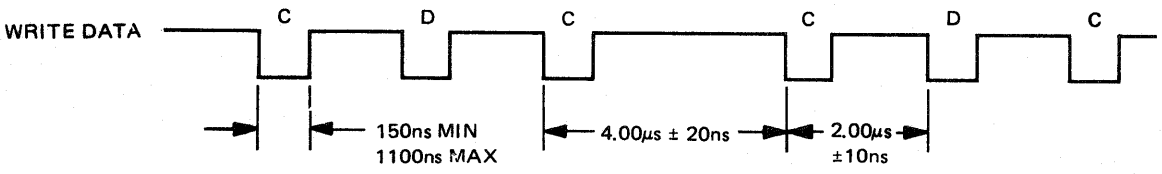
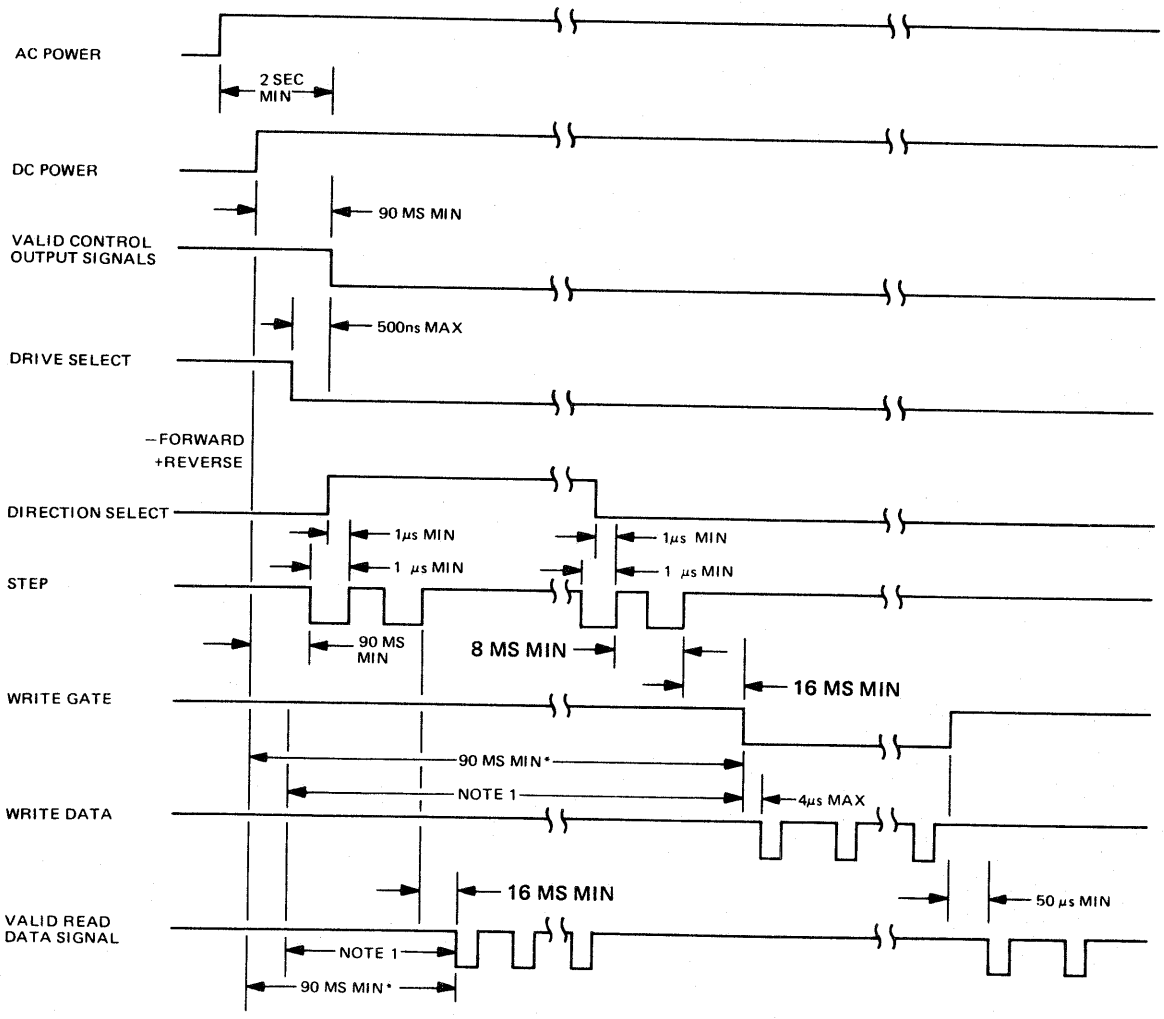


Figure 7. Write Data Timing



* 2 SECONDS IF AC AND DC POWER ARE APPLIED AT SAME TIME

NOTE 1: 35ms minimum delay must be introduced after Drive Select to allow for proper head load settling. If stepper power is to be applied independent of Head Load, then an 8ms minimum delay must be introduced to allow for stepper settling. See section 7 on optional customer installable features.

Figure 8. General Control and Data Timing Requirements

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4.0 ELECTRICAL INTERFACE

The interface of the SA800/801 Diskette drive can be divided into two categories:

1. Signal
2. Power

The following sections provide the electrical definition for each line.

Reference Figure 9 for all interface connections.

4.1 Signal Interface

The signal interface consists of two categories:

1. Control
2. Data transfer

All lines in the signal interface are digital in nature and either provide signals to the drive (input), or provide signals to the host (output), via interface connector P1/J1.

4.1.1 Input Lines

There are ten (10) signal input lines, eight (8) are standard and two (2) are user installable options (reference section 7).

The input signals are of two types, those intended to be multiplexed in a multiple drive system and those which will perform the multiplexing. The input signals to be multiplexed are:

1. Direction Select
2. Step
3. Write Data
4. Write Gate

The input signals which are intended to do the multiplexing are:

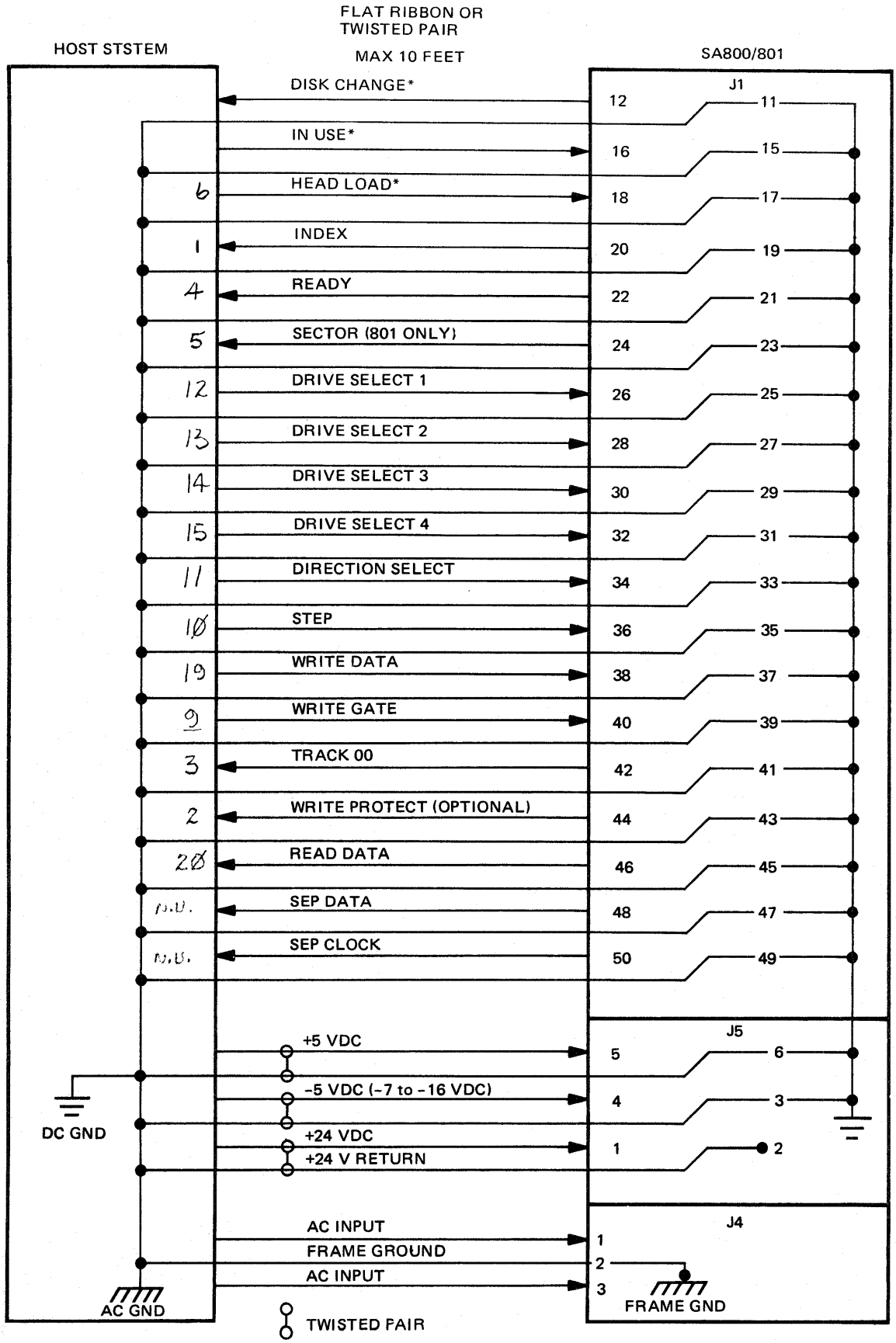
1. Drive Select 1
2. Drive Select 2
3. Drive Select 3
4. Drive Select 4

The input lines have the following electrical specifications. Reference Figure 10 for the recommended circuit.

True = Logical zero = Vin ±0.0V to +0.4V
@ Iin = 40 ma (max)

False = Logical one = Vin +2.5V to +5.25V
@ Iin = 0 ma (open)

Input Impedence = 150 ohms



NOTE: Not shown are 6 of the 9 Alternate I/O connections. The connections for these lines are on pins 2, 4, 6, 8, 10, and 14. Signal return for these lines are on pins 1, 3, 5, 7, 9 and 13 respectively. Reference section 7 for uses of these lines.

*These lines are alternate input/output lines and they are enabled by plugs. Reference section 7 for uses of these lines.

Figure 9. Interface Connections

4.1.1.1 Input Line Termination

The SA800/801 has been provided with the capability of terminating the four input lines, which are meant to be multiplexed, by jumpering traces. The four lines and their respective jumpering traces are:

1. Direction Select . . . . . Trace "T3"
2. Step. . . . . Trace "T4"
3. Write Data . . . . . Trace "T5"
4. Write Gate . . . . . Trace "T6"

In order for the drive to function properly, the last drive on the interface must have these four lines terminated. Termination of these four lines can be accomplished by either of two methods.

1. As shipped from the factory, jumpers are installed on the terminator posts T3, T4, T5, and T6. Remove these shorting plugs from all drives except the last one on the Interface.

2. External termination may be used provided the terminator is beyond the last drive. Each of the four lines should be terminated by using a 150 ohm, ¼ watt resistor, pulled up to +5 VDC.

4.1.1.2 Drive Select 1 - 4

Drive Select when activated to a logical zero level, activates the multiplexed I/O lines and loads the R/W head. In this mode of operation only the drive with this line active will respond to the input lines and gate the output lines.

Four separate input lines, Drive Select 1, Drive Select 2, Drive Select 3, and Drive Select 4, are provided so that up to four drives may be multiplexed together in a system and have separate Drive Select lines. Traces 'DS1', 'DS2', 'DS3', and 'DS4' have been provided to select which Drive Select line will activate the interface signals for a unique drive. As shipped from the factory, a shorting plug is installed on 'DS1'. To select another Drive Select line, this plug should be moved to the appropriate 'DS' pin. For additional methods of selecting drives, see section 7.1.

4.1.1.3 Direction Select

This interface line is a control signal which defines direction of motion the R/W head will take when the Step line is pulsed. An open circuit or logical one defines the direction as "out" and if a pulse is applied to the Step line the R/W head will move away from the center of the disk. Conversely, if this input is shorted to ground or a logical zero level, the direction of motion is defined as "in" and if a pulse is applied to the step line, the R/W head will move towards the center of the disk.

4.1.1.4 Step

This interface line is a control signal which causes the R/W head to move with the direction of motion as defined by the Direction Select line.

The access motion is initiated on each logical zero to logical one transition, or the trailing edge of the signal pulse. Any change in the Direction Select line must be made at least 1μs before the trailing edge of the Step pulse. Refer to Figure 3 for these timings.

4.1.1.5 Write Gate

The active state of this signal, or logical zero, enables Write Data to be written on the diskette. The inactive state, or logical one, enables the read data logic (Separated Data, Separated Clock, and Read Data) and stepper logic. Refer to Figure 6 for timings.

4.1.1.6 Write Data

This interface line provides the data to be written on the diskette. Each transition from a logical one level to a logical zero level, will cause the current through the R/W head to be reversed thereby writing a data bit. This line is enabled by Write Gate being active. Refer to Figure 7 for timings.

4.1.1.7 Head Load (Alternate Input)

This customer installable option, when enabled by jumpering Trace 'C' and activated to a logical zero level and the diskette access door is closed, will load the R/W head load pad against the diskette. Refer to section 7 for uses and method of installation.

4.1.1.8 In Use (Alternate Input)

This customer installable option, when enabled by jumpering Trace 'D' and activated to a logical zero level will turn on the Activity LED in the door push button. This signal is an "OR" function with Drive Select. Refer to section 7.8 for uses and method of installation.

4.1.2 Output Lines

There are six (6) standard and one (1) optional output lines from the SA800, and eight (8) output lines from the SA801. Also, there is one (1) Alternate Output available from the drive. The output signals are driven with an open collector output stage capable of sinking a maximum of 40 ma at a logical zero level or true state with a maximum voltage of 0.4V measured at the driver. When the line driver is in a logical one or false state the driver is off and the collector current is a maximum of 250 microamperes.

Refer to Figure 10 for the recommended circuit.

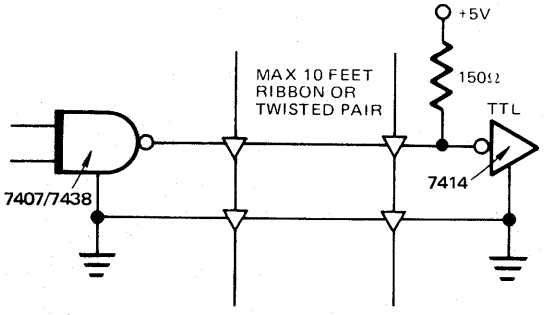


Figure 10. Interface Signal Driver/Receiver

4.1.2.1 Track 00

The active state of this signal, or a logical zero indicates when the drives R/W head is positioned at track zero (the outer most track) and the access circuitry is driving current through phase one of the stepper motor. This signal is at a logical one level, or false state, when the selected drives R/W head is not at track 00.

4.1.2.2 Index

This interface signal is provided by the drive once each revolution of the diskette (166.67ms) to indicate the beginning of the track. Normally this signal is a logical one and makes the transition to the logical zero level for a period of 1.7ms (0.4ms on SA801) once each revolution. The timing for this signal is shown in Figure 11.

To correctly detect Index at the control unit, Index should be false at Drive Select time, that is, the CU should see the transition from false to true after the drive has been selected.

For additional methods of detecting Index, refer to section 7.6.

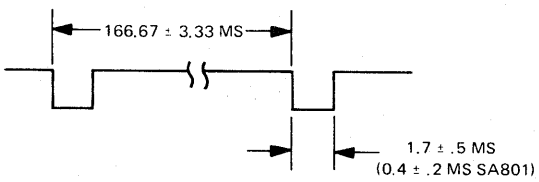


Figure 11. Index Timing

4.1.2.3 Sector (SA801 only)

This interface signal is provided by the drive 32 times each revolution. Normally, this signal is a logical one and makes the transition to a logical zero for a period of 0.4ms each time a sector hole on the Diskette is detected. Figure 12 shows the timing of this signal and its relationship to the Index pulse.

For additional methods of detecting Sector refer to section 7.7.

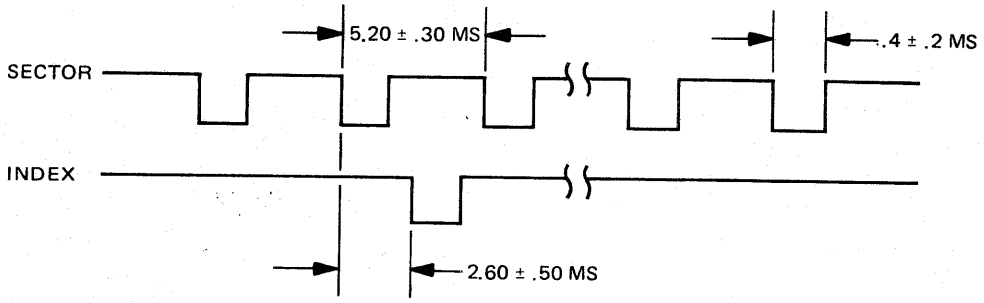


Figure 12. Sector Timing

4.1.2.4 Ready

This interface signal indicates that two (2) index holes have been sensed after properly inserting a diskette and closing the door, or that two index holes have been sensed following the application of +5V power to the drive.

For additional methods of using the Ready line, refer to section 7.5.

4.1.2.5 Read Data

This interface line provides the "raw data" (clock and data together) as detected by the drive electronics. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference Figure 5 for the timing and bit shift tolerance within normal media variations.

4.1.2.6 Sep Data

This interface line furnishes the data bits as separated from the "raw data" by use of the internal data separator. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference Figure 5 for the timing. This line is available on the SA800/801 Model 1 only.

4.1.2.7 Sep Clock

This interface line furnishes the clock bits as separated from the "raw data" by use of the internal data separator. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference Figure 5 for the timing. This line is available on the SA800/801 Model 1 only.

4.1.2.8 Write Protect (Optional on SA800)

This interface signal is provided by the drive to give the user an indication when a Write Protected Diskette is installed. The signal is logical zero level when it is protected. Under normal operation, the drive will inhibit writing with a protected diskette installed in addition to notifying the interface.

For other methods of using Write Protect, refer to section 7.9.

4.1.2.9 Disk Change (Alternate Output)

Reference section 7.10.

4.1.3 Alternate I/O Pins

These interface pins have been provided for use with customer installable options. Refer to section 7 for methods of use.

4.2 Power Interface

The SA800/801 Diskette Storage Drive requires both AC and DC power for operation. The AC power is used for the spindle drive motor and the DC power is used for the electronics and the stepper motor.

4.2.1 AC Power

The AC power to the drive is via the connector P4/J4 located to the rear of the drive and below the AC motor capacitor. The P4/J4 pin designations are outlined below for standard as well as optional AC power.

P4 PIN	60 Hz		50 Hz	
	115 V (Standard)	208/230 V	110 V	220 V
1	85-127 VAC	170-253 VAC	85-127 VAC	170-253 VAC
2	Frame Gnd	Frame Gnd	Frame Gnd	Frame Gnd
3	85-127 V Rtn	170-253 V Rtn	85-127 V Rtn	170-253 V Rtn
MAX CURRENT	0.5 Amps	0.4 Amps	0.6 Amps	0.4 Amps
FREQ TOLERANCE	±0.5 Hz		±0.5 Hz	

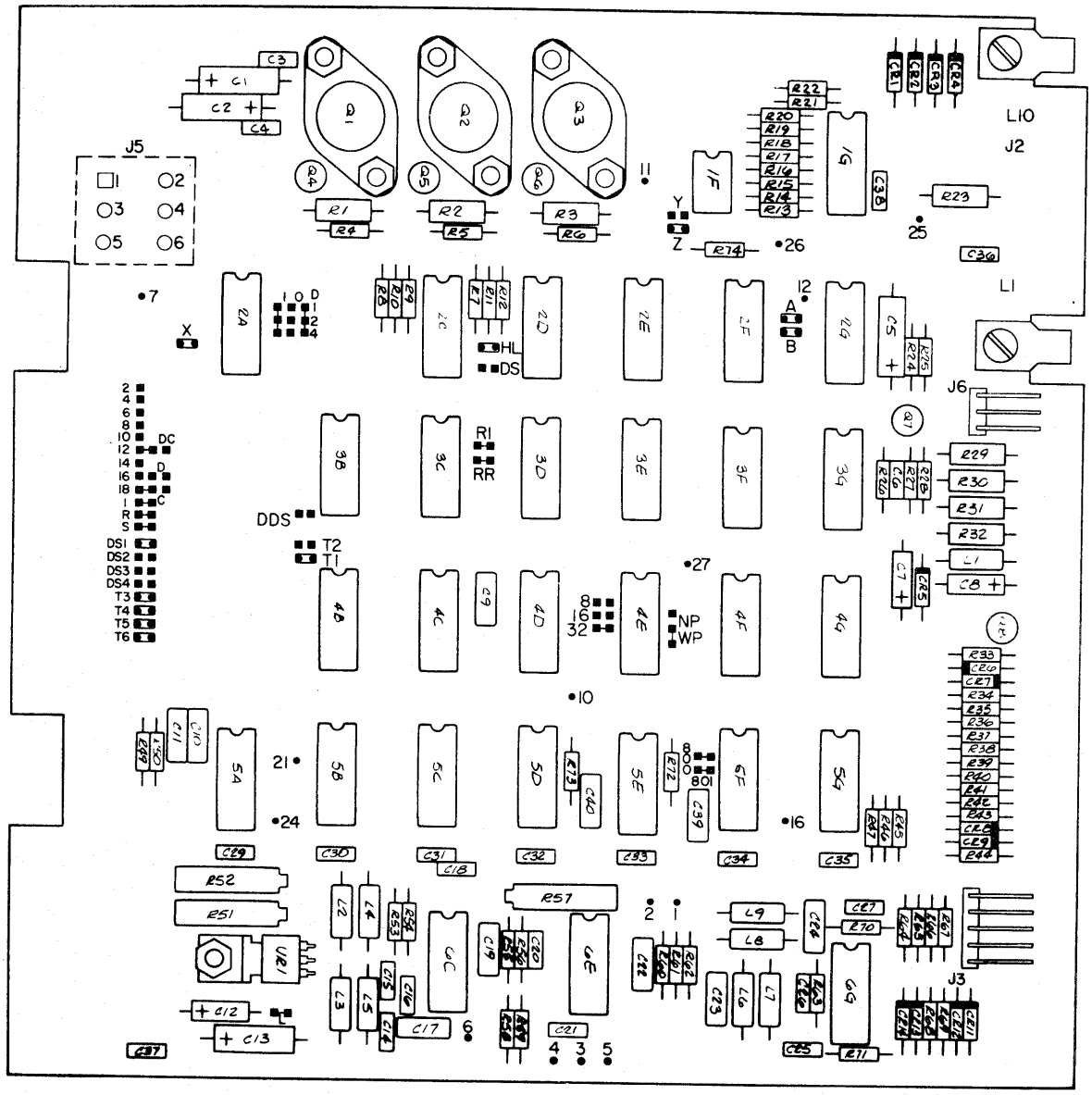
4.2.2 DC Power

DC power to the drive is via connector P5/J5 located on non-component side of PCB near the P4 connector. The three DC voltages and their specifications along with their P5/J5 pin designators, are outlined below.

P5 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (p to p)
1	+24 VDC	±1.2 VDC	1.7 A Max** 1.3 A Typ	100 mv
2	+24 V Return*			
3	- 5 V Return			
4	- 5 VDC	±0.25 VDC	0.07 A Max 0.05 A Typ	50 mv
	Optional - 7 to -16 VDC (Cut Trace 'L')	NA	0.10 A Max 0.07 A Typ	NA
5	+ 5 VDC	±0.25 VDC	1.0 A Max 0.8 A Typ	50 mv
6	+ 5 V Return			

*The +24 VDC power requires a separate ground return line. It, and all other DC grounds must be connected together near the power supply. One line from this common DC connection must go to one common Frame Ground connection.

**If either customer installable option described in sections 7.2 and 7.4 are used, the current requirement for the +24 VDC is a multiple of the maximum +24V current times the number of drives on the line.



■ Jumper Plug Installed as Shipped

• Test Point

Figure 20 SA800/801 PCB Component Locations

7.0 CUSTOMER INSTALLABLE OPTIONS

The SA800/801 can be modified by the user to function differently than the standard method as outlined in sections 3 and 4. These modifications can be implemented by adding or deleting traces and by use of the Alternate I/O pins. Some traces are capable of being connected by use of a shorting plug, Shugart P/N 15648 or AMP P/N 530153-2. This section will discuss a few examples of modifications and how to install them. The examples are:

1. Drive Select one to eight drives.
2. Select drive without loading head or enabling stepper.
3. Select drive and enable stepper without loading head.
4. Load head without selecting drive or enabling stepper.
5. Radial Ready.
6. Radial Index/Sector.
7. Eight, 16, or 32 Sector option.
8. In Use (Activity L.E.D.) optional input.
9. Write Protect options.

Tabulated below are the trace options with the condition of the trace as it is shipped from the factory. Figure 20 shows the location of these traces on the PCB.

CUSTOMER CUT/ADD TRACE OPTIONS

TRACE DESIGNATOR	DESCRIPTION	SHIPPED FROM FACTORY	
		OPEN	SHORT
T3,T4,T5,T6	Terminations for Multiplexed Inputs		Plugged
T1	Terminator for Srive Select		Plugged
T2	Spare Terminator for Radial Head Load	X	
DS1,DS2,DS3,DS4	Drive Select Input Pins	X	DS1 is Plugged
RR	Radial Ready		X
RI	Radial Index and Sector		X
R,I,S,	Ready, Index, Sector Alternate Output Pads		X
HL	Stepper Power From Head Load		Plugged
DS	Stepper Power From Drive Select	X	
WP	Inhibit Write When Write Protected		X
NP	Allow Write When Write Protected	X	
8,16,32,	8, 16, 32 Sectors (SA801 Only)	8 & 16	32
D	Alternate Input-In Use	X	
2,4,6,8,10,12,14,16,18	Nine Alternate I/O Pins	X	
D1,D2,D4,DDS	Customer Installable Decode Drive Select Option	X	
A,B,X	Radial Head Load		Plugged
C	Alternate Input-Head Load	X	
Z	In Use from Drive Slect		Plugged
Y	In Use from HD LD	X	
DC	Alternate Output-Disk Change	X	

7.1 Drive Select – One To Eight Drives

This customer installed option allows up to eight drives to be multiplexed together. This method of drive selection uses a binary address to select a drive.

To install this feature on a standard drive, the following traces should be added or deleted:

1. Add a 74L85, 4 bit comparator, into position 2B on PCB.
2. Connect trace 'DDS'.
3. Insure traces 'DS1' - 'DS4' are unplugged.
4. Jumper traces 'D1', 'D2', and 'D4' according to table below for the address of each drive.

ADDRESS	TRACE		
	D1	D2	D4
0 A	0	0	0
1 B	1	0	0
2 C	0	1	0
3 D	1	1	0
4 E	0	0	1
5 F	1	0	1
6 G	0	1	1
7 H	1	1	1

The four Drive Select lines are to be used for addressing the drives. Pin 26 is used as Drive Select enable and pins 28 (binary 1), 30 (binary 2), and 32 (binary 4) are the address lines. The table below shows the logical state each line must be at to select each of the drives.

DRIVE	INTERFACE PIN			
	26	28	30	32
0	0	1	1	1
1	0	0	1	1
2	0	1	0	1
3	0	0	0	1
4	0	1	1	0
5	0	0	1	0
6	0	1	0	0
7	0	0	0	0

Figure 21 illustrates the circuitry.

The four drive select lines must be terminated externally.

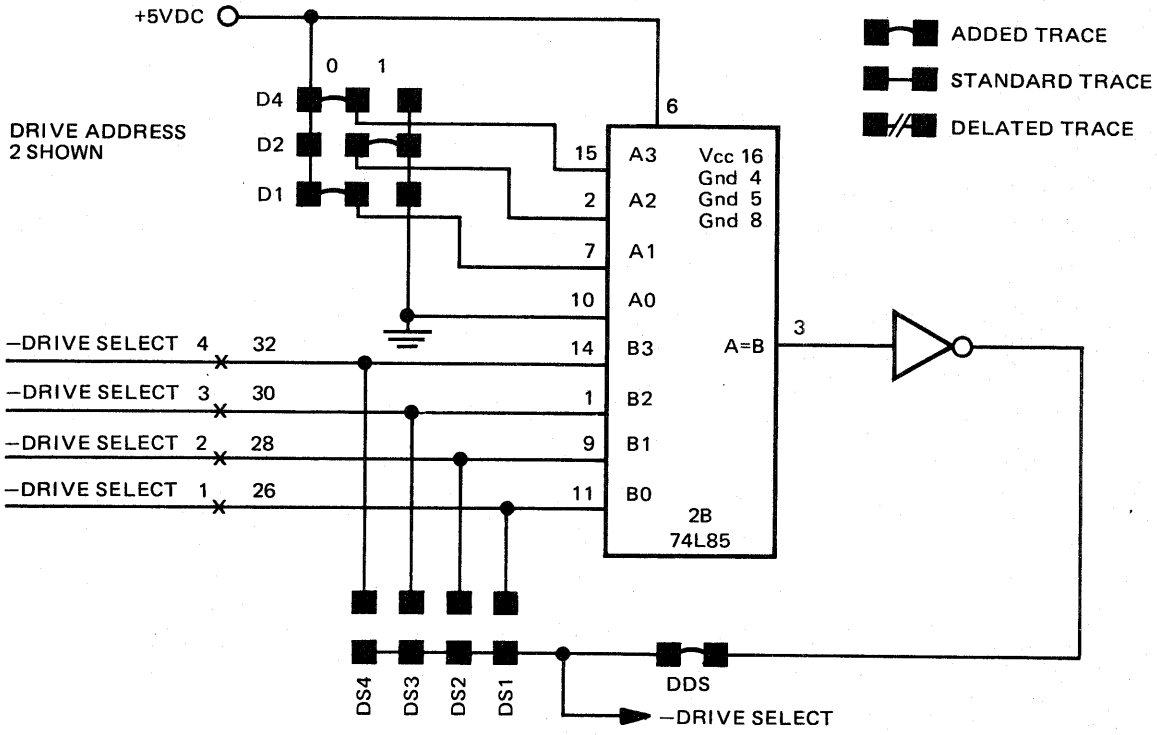


Figure 21. Drive Select Circuitry

7.2 Select Drive Without Loading Head Or Enabling Stepper Motor

This option would be advantageous to the user who requires a drive to be selected at all times. Normally, when a drive is selected, its head is loaded and the stepper motor is energized. The advantage of this option would be that the output control signals could be monitored (with the exception of Track Zero, which requires the stepper to be energized) while the head was unloaded thereby extending the head and media life. When the system requires the drive to perform a Read, Write, or Seek, the controller would activate the Head Load line (pin 18) which in turn would load the head and energize the stepper motor. After the Head Load line is activated, a 35 ms delay must be introduced before Write Gate and Write Data may be applied or before Read Data is valid.

To install this option on a standard drive, the following traces should be added or deleted:

1. Jumper trace 'T2'.
2. Remove jumper from trace 'X'.
3. Jumper trace 'C'.

Figure 22 illustrates the circuitry.

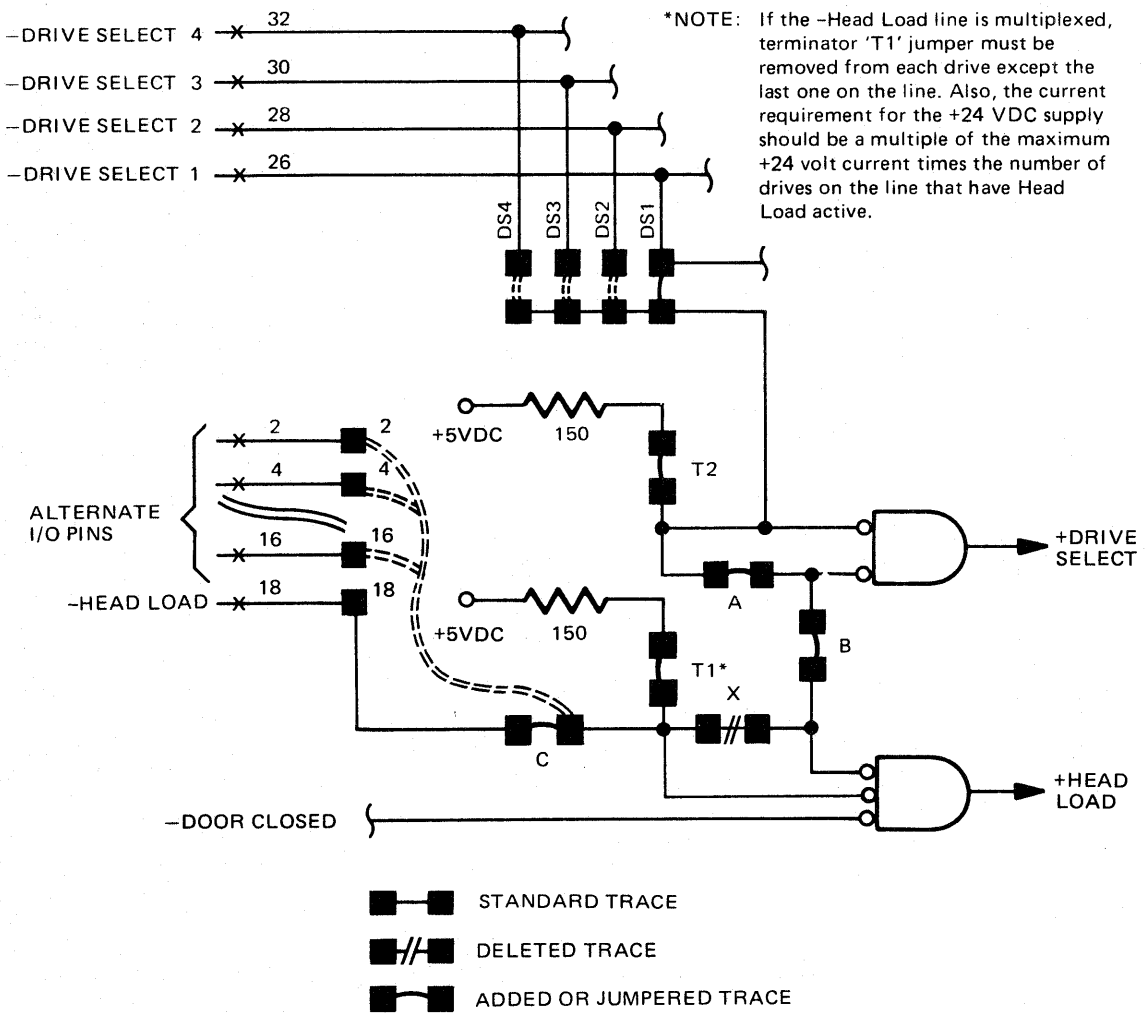


Figure 22. Select Drive Without Loading Head Circuit

8.0 OPERATION PROCEDURES

The SA800/801 was designed for ease of operator use to facilitate a wide range of operator oriented applications. The following section is a guide for the handling and error recovery procedures on the diskette and diskette drive.

8.1 Diskette Loading and Handling

The diskette is a flexible disk enclosed in a plastic jacket. The interior of the jacket is lined with a wiping material to clean the disk of foreign material. Figure 33 shows the proper method of loading a diskette in the SA800/801 Diskette Storage Drive. To load the diskette, depress latch, insert the diskette with the label facing out. (See Figure 33.) Move the latch handle to the left to lock diskette on drive spindle. The diskette can be loaded or unloaded with all power on and drive spindle rotating.

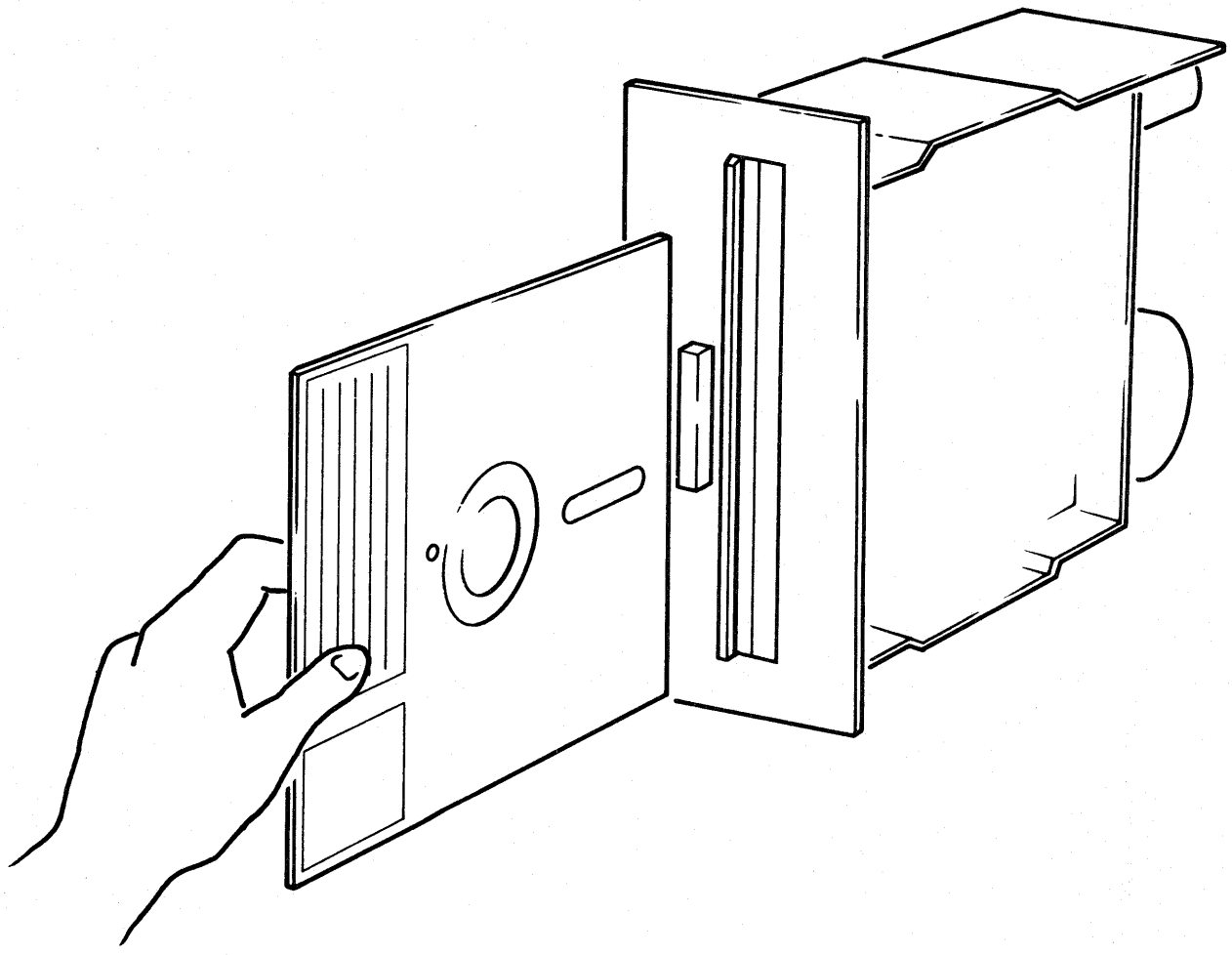


Figure 33. Loading SA800/801

When removed from the drive, the diskette is stored in an envelope. To protect the diskette, the same care and handling procedures specified for computer magnetic tape apply. These precautionary procedures are as follows:

1. Return the diskette to its storage envelope whenever it is removed from file.
2. Keep cartridges away from magnetic fields and from ferromagnetic materials which might become magnetized. Strong magnetic fields can distort recorded data on the disk.
3. Replace storage envelopes when they become worn, cracked or distorted. Envelopes are designed to protect the disk.
4. Do not write on the plastic jacket with a lead pencil or ball-point pen. Use a felt tip pen.
5. Heat and contamination from a carelessly dropped ash can damage the disk.
6. Do not expose diskette to heat or sunlight.
7. Do not touch or attempt to clean the disk surface. Abrasions may cause loss of stored data.

8.2 SA101 Write Protect

The SA101 has the capability of being write protected. The write protect feature is selected by the hole in the SA101. When the hole is open it is protected; when covered, writing is allowed. The hole is closed by placing a tab over the front of the hole, and the tab folded over covering the rear of the hole. The Diskette can then be write protected by removing the tab. See Figure 34.

8.3 SA100 Write Protect

The SA100 or IBM Diskettes are not manufactured with a write protect hole punched out as are the SA101 Diskettes. To Write-Protect one of these diskettes, a hole must be punched out as specified in Figure 35. The operation of the write protect is that which is outlined in paragraph 8.2.

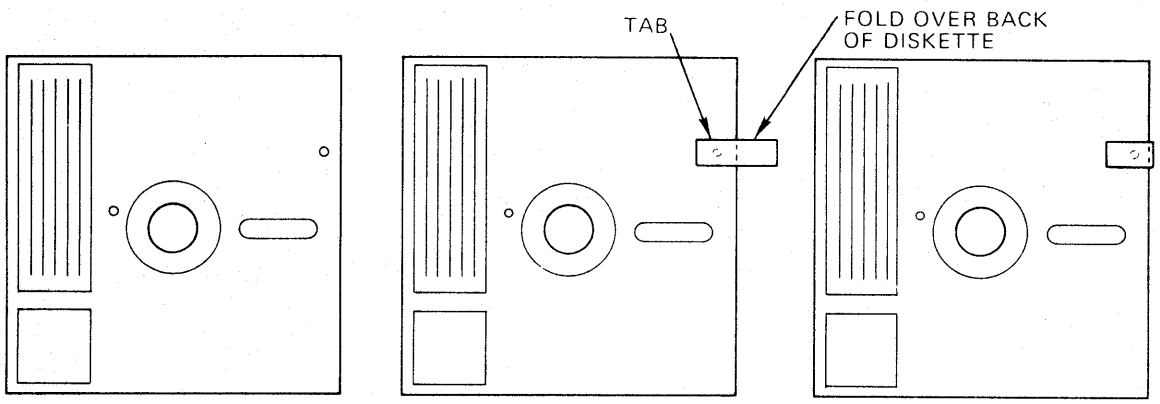


Figure 34. Diskette Write Protected

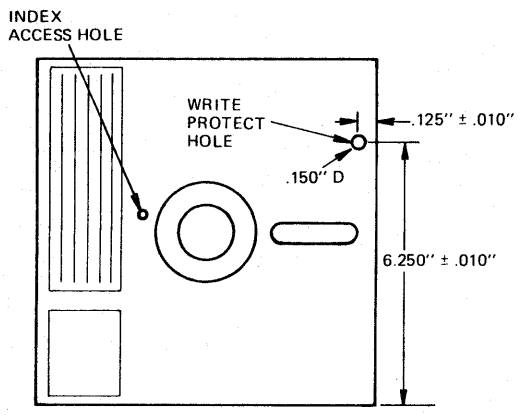
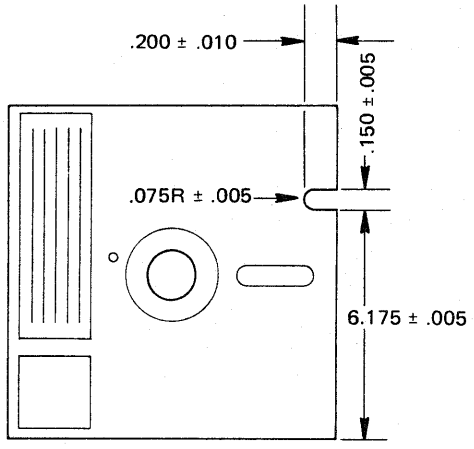


Figure 35. Write Protect Hold Specifications



Write Inhibit Notch (Optional)

LOGIC MANUAL DRIVE SN _____

INDEX

AA001	INDEX
AB010	PCB TRACE AND TEST POINT LOCATIONS
DA010	READ/WRITE/INDEX/SECTOR
DA020	STEPPER CONTROL
DA030	DETECTORS
DA040	MOTORS SOLENOID SWITCH

TABLE III
CUSTOMER CUT TRACE OPTIONS

DESIGNATOR	DESCRIPTION	SHIPPED FROM FACTORY OPEN	SHORT
T3,T4,T5 & T6	TERMINATIONS FOR MULTIPLEXED INPUTS		[1] X
T2	SPARE TERMINATOR FOR RADIAL HEAD LOAD	X	
TI	TERMINATION FOR DRIVE SELECT		[1] X
DSI	DRIVE SELECT INPUT – ALTERNATE PINS: DS2,DS3,DS4		[1] X
RR	RADIAL READY		X
RI	RADIAL INDEX AND SECTOR		X
R,I,S	READY, INDEX, SECTOR ALTERNATE OUTPUT PROVISION		X
A,B,X	RADIAL HEAD LOAD		[1] X
HL	STEPPER POWER FROM HD LD		[1] X
DS	STEPPER POWER FROM DRIVE SELECT	X	
WP	INHIBIT WRITE WHEN WRITE PROTECTED		X
NP	ALLOW WRITE WHEN WRITE PROTECTED	X	
8,16,32	8,16 OR 32 SECTORS		
D	ALTERNATE INPUT – IN USE	X	
2,4,6,8,10,12,14,16,18	NINE ALTERNATE I/O PINS	X	
DI, D2, D4, DDS	CUSTOMER INSTALLABLE DECODE DRIVE SELECT OPTION	X	
C	ALTERNATE INPUT – HEAD LOAD	X	
Z	INUSE LED FROM DRIVE SELECT		[1] X
Y	INUSE LED FROM HD LD	X	
DC	ALTERNATE OUTPUT – DISK CHANGE	X	

FACTORY CUT TRACE OPTIONS AND HISTORY CHART

L	-5 OR -7 TO -16V	SEE TABLE II
800	INDEX ONLY (800)	SEE TABLE II
801	INDEX AND SECTOR(801)	SEE TABLE II

[1] OPEN TRACE WITH SHORTING PLUG INSTALLED.

TABLE I
OPTIONAL FEATURES

PCB ASM NO.	OPTIONAL FEATURES -5V	-7 TO -16V	DATA SEP	SECTOR SEP
25102	X			
25103		X		
25104	X		X	
25105		X	X	
25106	X		X	X
25107		X	X	X

WRITE PROTECT CAN BE ORDERED WITH ANY OF THE ABOVE

TABLE II
FACTORY CUT TRACE OPTIONS

PCB ASM NO	TRACE "L"	TRACE "801"	TRACE "800"
25102	SHORTED	OPEN	SHORTED
25103	OPEN	↑	↑
25104	SHORTED	↓	↓
25105	OPEN	OPEN	SHORTED
25106	SHORTED	SHORTED	OPEN
25107	OPEN	SHORTED	OPEN

LOGIC MANUAL P/N 50590-1

PART NO 50591-0

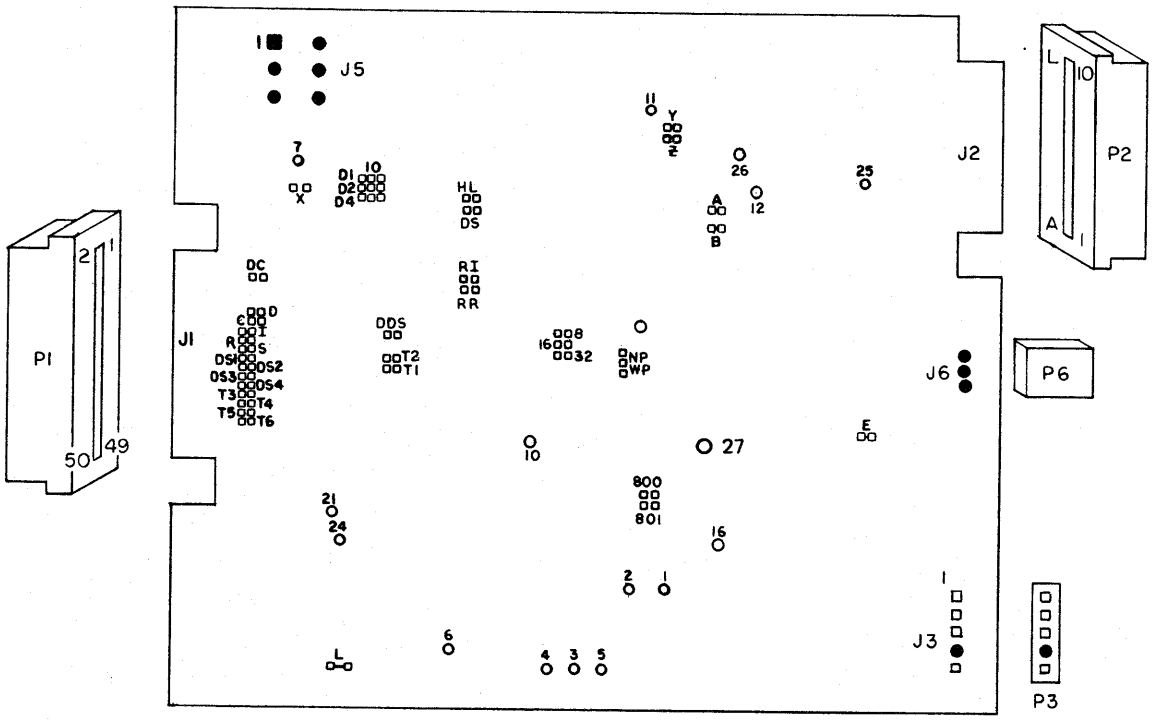
10-31

AA001

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY DATE	NO.	SHUGART ASSOCIATES
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	6-75	0398	TITLE INDEX
	LINEAR ±.XX	1-76	0509	DETAIL RELEASED FOR ASSEMBLY 6-6-75
CASE DEPTH	±.XXX			DESIGN 50590
HARDNESS	ANGULAR±			APPRO SHEET 1 OF 1 6-7 6-75
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX / INSIDE MAX			C SCALE — DOC CODE OD PART NO. 50591-0 REV/EC 0509

PART NO. 50592-0

10-32

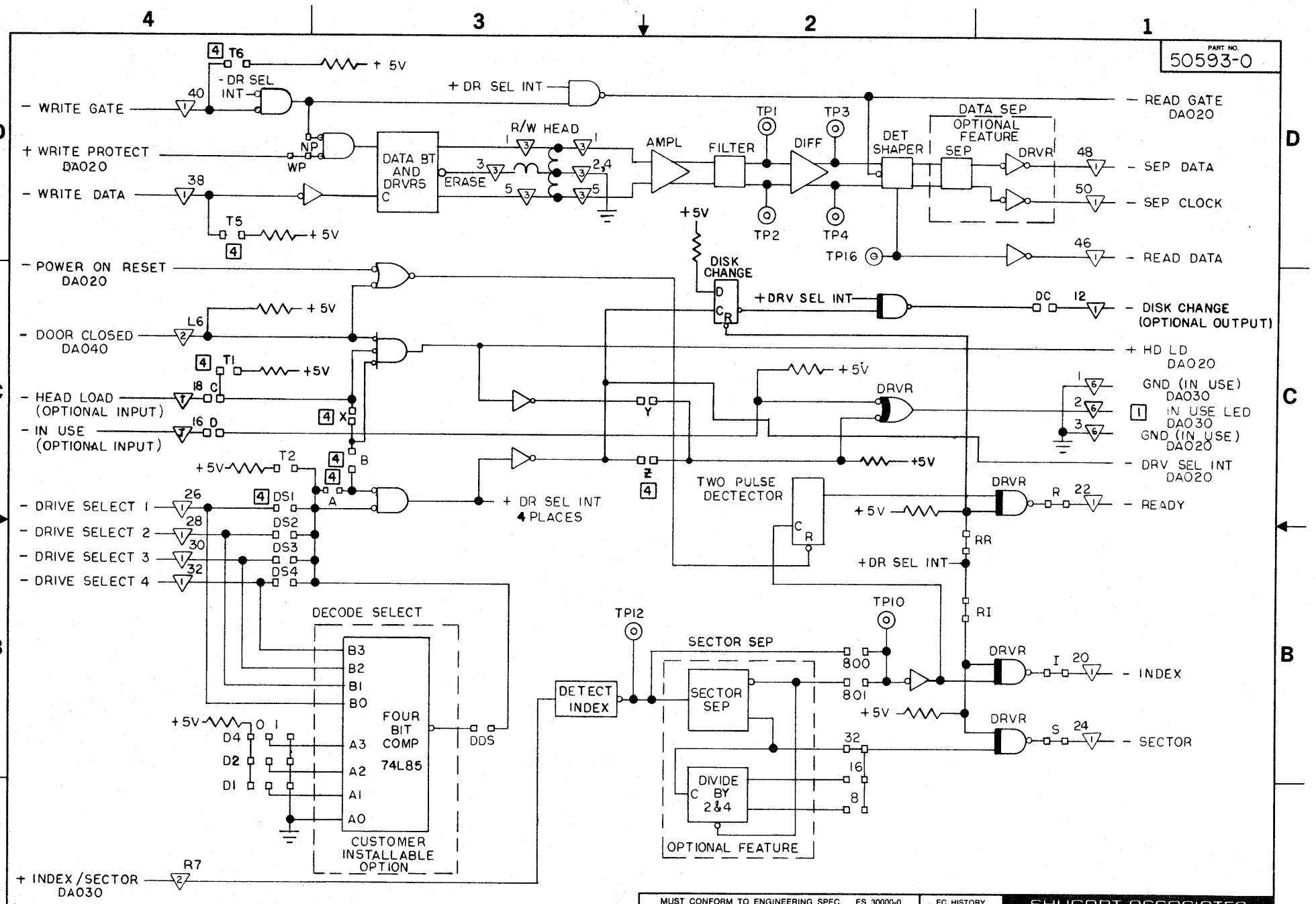


TEST POINTS	
TP1 & TP2	FILTERED READ SIGNAL
TP3 & TP4	DIFFERENTIATED READ SIGNAL
TP5, TP6, TP7	SIGNAL GROUND
TP10	−INDEX (TTL)
TP11	−LOAD HEAD (TTL)
TP12	−DETECTED INDEX/SECTOR HOLES(TTL)
TP16	+READ DATA (TTL)
TP21	DATA SEPARATOR TIME t1 (TTL)
TP24	DATA SEPARATOR TIME t2(TTL)
TP25	+WRITE PROTECT
TP26	+DETECTED TRACK ZERO (TTL)
TP27	+GATED STEP PULSE (TTL)

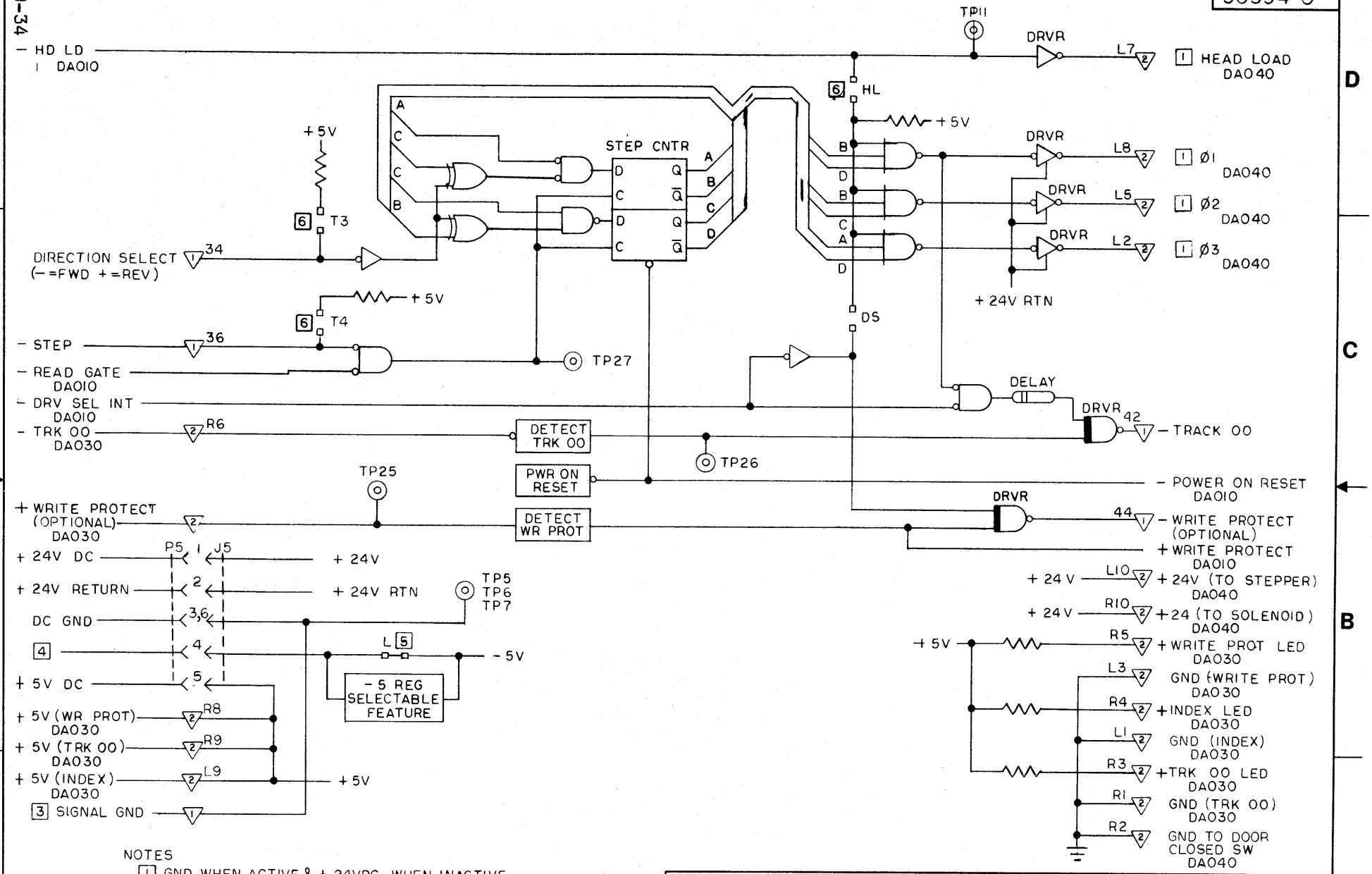
NOTES:
1. ○–○/○○ DENOTES CUT TRACE/JUMPER OPTION.
2. ○ DENOTES TEST POINTS.

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0			EC HISTORY		SHUGART ASSOCIATES				
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED		DATE	NO.	TITLE	PCB TRACE AND TEST POINT LOCATION			
			6-75	0398					
	LINEAR ±.XX ±.XXX		1-76	0509	DETAIL	[illegible]	6-6-75	RELEASED FOR ASSEMBLY	
CASE DEPTH					DESIGN			50590	
HARDNESS	ANGULAR±				APPRO	[illegible]	6-75	SHEET | OF |	
SURFACE TREATMENT ES	CORNERS EDGES BROKEN	OUTSIDE MAX			C	SCALE —	DOC CODE OD	PART NO. 50592-0	REV/EC 0509
		INSIDE MAX							

AB010


PART NO. 50593-0
- WRITE GATE
+ WRITE PROTECT DA020
- WRITE DATA
- DR SEL INT
+ DR SEL INT
- READ GATE DA020
DATA BT AND DRVRS
R/W HEAD
ERASE
AMPL
FILTER
DIFF
DET SHAPER
DATA SEP OPTIONAL FEATURE
SEP
DRVR
- SEP DATA
- SEP CLOCK
- READ DATA
TP1
TP2
TP3
TP4
TP16
+5V
DISK CHANGE
+DRV SEL INT
- DISK CHANGE (OPTIONAL OUTPUT)
- POWER ON RESET DA020
- DOOR CLOSED DA040
- HEAD LOAD (OPTIONAL INPUT)
- IN USE (OPTIONAL INPUT)
+ HD LD DA020
GND (IN USE) DA030
IN USE LED DA030
GND (IN USE) DA020
- DRV SEL INT DA020
TWO PULSE DECTECTOR
- DRIVE SELECT 1
- DRIVE SELECT 2
- DRIVE SELECT 3
- DRIVE SELECT 4
+ DR SEL INT 4 PLACES
- READY
RR
RI
DECODE SELECT
FOUR BIT COMP 74L85
CUSTOMER INSTALLABLE OPTION
DDS
TP12
TP10
SECTOR SEP
DETECT INDEX
800
801
DIVIDE BY 2&4
OPTIONAL FEATURE
- INDEX
- SECTOR
+ INDEX/SECTOR DA030
NOTES:
1. GND WHEN INACTIVE AND + 1.5VDC WHEN ACTIVE
2. CONNECTOR SYMBOL REFERENCE ▽=J1, ▽=J2, ▽=J3, ▽=J6
3. ALL ODD NUMBERED PINS ON J1 CONNECTOR ARE GROUND.
4. SHORTING PLUG INSTALLED.
DA010
10-33
MUST CONFORM TO ENGINEERING SPEC. ES 30000-0
EC HISTORY
SHUGART ASSOCIATES
TITLE READ/WRITE/INDEX/SECTOR
RELEASED FOR ASSEMBLY
50590
SCALE
DOC CODE OD
PART NO. 50593-0
REV/EC 0509

PART NO. 50594-0



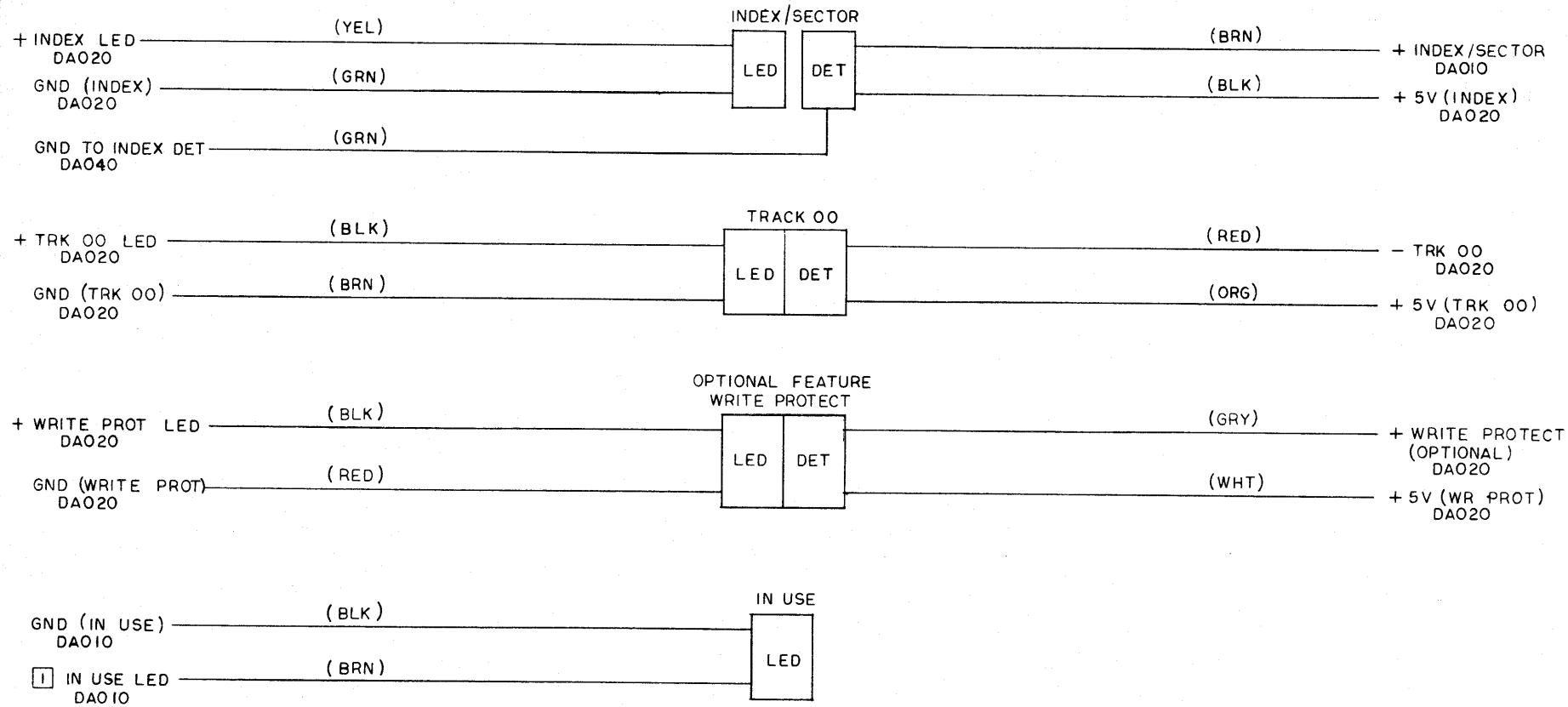
NOTES

1. GND WHEN ACTIVE & + 24VDC WHEN INACTIVE
2. CONNECTOR SYMBOL REFERENCE ▽1=J1, ▽2=J2, ▽5=J5.
3. ALL ODD NUMBERED PINS ON J1 CONNECTOR ARE GROUND.
4. −5V OR −7V TO −16V SELECTABLE FEATURE.
5. CUT TRACE L FOR −7V TO −16V INPUT AT P5-4. SEE PAGE AA001, TABLE II
6. SHORTING PLUG INSTALLED.

DA020

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY		SHUGART ASSOCIATES			
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.	TITLE	STEPPER CONTROL		
	LINEAR ±.XX ±.XXX	6-75	0398	DETAIL	G.W.	6-6-75	RELEASED FOR ASSEMBLY
CASE DEPTH		1-76	0509	DESIGN			50590
HARDNESS	ANGULAR±			APPRO	G.R.T	6-75	SHEET 1 OF 1
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX			C	SCALE —	DOC CODE OD	PART NO. 50594-0 REV/EC 0509

PART NO. 50595-0



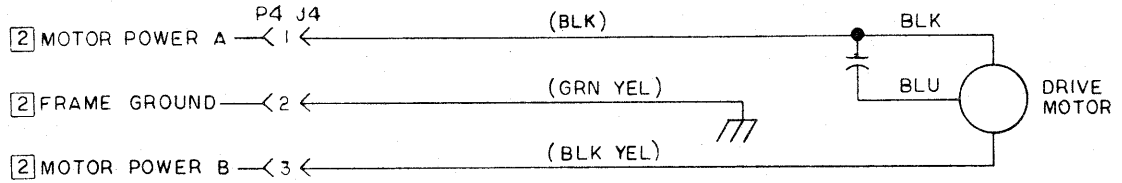
NOTES:
[1] GND WHEN INACTIVE AND +1.5VDC WHEN ACTIVE

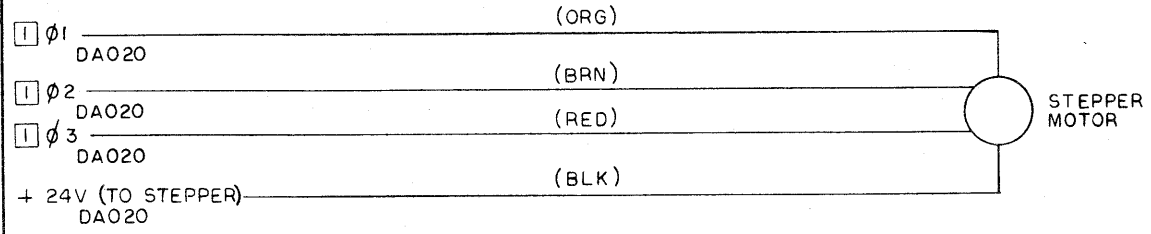
10-35

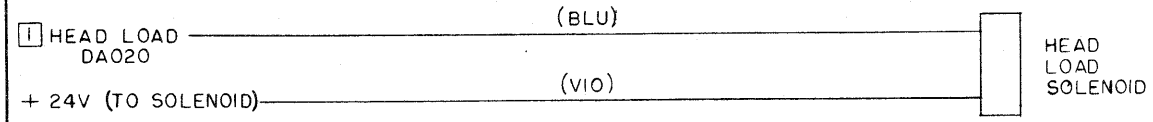
DA030

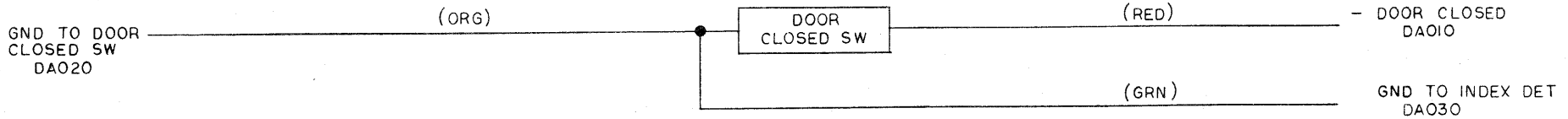
MUST CONFORM TO ENGINEERING SPEC. ES 30000-0			EC HISTORY		SHUGART ASSOCIATES
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED		DATE	NO.	TITLE: DETECTORS
	LINEAR ±.XX		6-75	0398	
CASE DEPTH	±.XXX				DETAIL 6.C.R 6-6-75 RELEASED FOR ASSEMBLY
HARDNESS	ANGULAR±				DESIGN 50590
SURFACE TREATMENT ES	CORNERS EDGES BROKEN	OUTSIDE MAX			APPRO 6-6-7 6-75 SHEET 1 OF 1
		INSIDE MAX			C SCALE — DOC CODE OD PART NO. 50595-0 REV/EC 0398

PART NO. 50596-0









NOTES:
[1] GND WHEN ACTIVE & +24V WHEN INACTIVE.
[2] 115 OR 230 VAC

DA040

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY		SHUGART ASSOCIATES	
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.	TITLE	MOTORS/SOLENOID/SWITCH
		6-75	0398		
	LINEAR ±.XX	1-75	0509	DETAIL	RELEASED FOR ASSEMBLY
CASE DEPTH	LINEAR ±.XXX			DESIGN	50590
HARDNESS	ANGULAR±			APPRO	SHEET 1 OF 1
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX			C	SCALE — DOC CODE OD PART NO. 50596-0 REV/EC 0509
	CORNERS EDGES BROKEN INSIDE MAX				

TEXAS ELECTRONIC INSTRUMENTS INC

ENGINEERING ORDER

E.O. NO.	SHT
985	1 OF 1

DOCUMENT TITLE

JUMPER OPTION CHANGE SA800

DOCUMENT NO.	REV

CHANGE (INCL ON DOCUMENT) (NOT INCL ON DOCUMENT)

PROJ NO.

TYPE E.O.					
✓	NEW DOCUMENT RELEASE (ND)		DISPOSITION OF PARTS	✓	
	REVISED DOCUMENT (RD)	✓	REWORK	✓	
	ADVANCE NOTICE (AN)	✓	SCRAP		
	VARIATION APPROVAL (VA)		CANCEL		
			STOP WORK		

BY E. McCain DATE 4-19-78
CHK D. Harrison DATE 4-19-78
ENGR Wallace Berry DATE 4-19-78
APP [signature] DATE 4-19-78

DETAILED DESCRIPTION:

PURPOSE: Eliminate head load bounce without slowing disk copy speed.

CORRECTION: Jumper SA800 Drive as follows.

DRIVE "A"	DRIVE "B"	DRIVE "C" & DRIVE "D"
T1		are jumpered the same as "B"
T3		
T4	N.A	
T5		
T6		
C	C	
DS	DS	
Z	Z	
A	A	
L	L	
X	X	
800	800	

JUSTIFICATION: Jumpered to load head without selecting drive or enabling stepper motor.

Should be done on all drives in the field shipped before May 1978.

This jumper modification to be done on all disk drives starting April 19, 1978.

DISTRIBUTION / QTY	ENGRG	SHOP	PROCUREMENT	MANUAL		
						10-37

TEL FORM NO. 105

TEXAS ELECTRONIC INSTRUMENTS INC

ENGINEERING ORDER

E.O. NO	SHT
1047	1 OF 1

DOCUMENT TITLE	DFD SA800 SA850	DOCUMENT NO.	REV
PT 212 or PT 412		13686-10	

CHANGE: (INCL ON DOCUMENT) (NOT INCL ON DOCUMENT)

PROJ NO.

TYPE E.O.					
✓	NEW DOCUMENT RELEASE (NDR)		DISPOSITION OF PARTS	✓	
	REVISED DOCUMENT (RDR)		REWORK		
	ADVANCE NOTICE (ANR)		SCRAP		
	VARIATION APPROVAL (VA)		CANCEL		
			STOP WORK		

BY W. Berry DATE 9/6/78
CHK _____ DATE _____
ENGR E. McLain DATE 9-12-78
APP _____ DATE _____

DETAILED DESCRIPTION:

DRIVE	A	B	C	D
T1				
T2		T2	T2	T2
T3				
T4				
T5				
T6				
C		C	C	C
DS		DS	DS	DS
Z		Z	Z	Z
A		A	A	A
L		L	L	L
X		X	X	X
800		800	800	800
		DS2	DS4	DS1

NOTE: FOR USE WITH T-DOS VERSION 1.42

JUSTIFICATION: SA850 DRIVES WILL NO LONGER HAVE THE MULTIPLEX OPTION; THEREFORE; WE WILL NO LONGER MULTIPLEX SA800 EFFECTIVE SEPTEMBER 6, 1978.

UPDATED 12/15/78

DISTRIBUTION/QTY	ENGRG	SHOP	PROCUREMENT			
						10-38